Jawaharlal Nehru Engineering Collage

Laboratory Manual

Electronics Devices and Circuits

For

Second Year Engineering Students
(Affiliated to Dr. B.A.T.U.,Lonere)

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MGM'S
Jawaharlal Nehru Engineering College
N-6, CIDCO, Aurangabad
Department of Electronics & Telecommunication

Vision of the Department:

To develop **GREAT** technocrats and to establish centre of excellence in the field of **Electronics and Telecommunications.**

- ***G***lobal technocrats with human values
- ***R***esearch and lifelong learning attitude
- ***E***xcellent ability to tackle challenges
- ***A***wareness of the needs of society
- ***T***echnical expertise

Mission of the Department:

1. To provide good technical education and enhance technical competency by providing good infrastructure, resources, effective teaching learning process and competent, caring and committed faculty.

2. To provide various platforms to students for cultivating professional attitude and ethical values.

3. Creating a strong foundation among students which will enable them to pursue their career choice.

Jawaharlal Nehru Engineering College

Technical Document

This technical document is a series of Laboratory manuals of Electronics and Telecommunication Department and is a certified document of Jawaharlal Nehru engineering College. The care has been taken to make the document error-free. But still if any error is found, kindly bring it to the notice of subject teacher and HOD.

Recommended by,

HOD

Approved by,

Principal

FOREWORD

It is my great pleasure to present this laboratory manual for second year engineering students for the subject of Electronic Devices & circuits to understand and visualize the basic concepts of various circuits using ICs. Electronic Devices & circuits cover basic concepts of electronics. This being a core subject, it becomes very essential to have clear theoretical and designing aspects.

This lab manual provides a platform to the students for understanding the basic concepts of electronic devices and circuits. This practical background will help students to gain confidence in qualitative and quantitative approach to electronic circuits.

Good Luck for your Enjoyable Laboratory Sessions.

H.O.D
ECT Dept

LABORATORY MANUAL CONTENTS

This manual is intended for the Second Year students of ECT branches in the subject of Electronic Devices & Circuits. This manual typically contains practical/ Lab Sessions related to Electronic Devices & Circuits covering various aspects related to the subject for enhanced understanding.

Students are advised to thoroughly go through this manual rather than only topics mentioned in the syllabus as practical aspects are the key to understanding and conceptual visualization of theoretical aspects covered in the books.

Good Luck for your enjoyable Laboratory Sessions.

SUBJECT INDEX:

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2. Lab Exercises

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2. To plot the drain characteristics of N-channel EMOSFET
3. To study the circuit of RC Phase Shift Oscillator & Determine the frequency of Oscillator
4. To study the circuit of Colpitts or LC Oscillator & Determine the frequency of Oscillator
5. To study a two stage RC Coupled Amplifier with negative feedback using transistor and plot the frequency response to calculate the bandwidth
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Dos and Don'ts in Laboratory :-

1. Do not handle any equipment before reading the instructions /Instruction manuals.
2. Read carefully the power ratings of the equipment before it is switched ON, whether ratings 230 V/50 Hz or 115V/60 Hz. For Indian equipment, the power ratings are normally 230V/50Hz. If you have equipment with 115/60 Hz ratings, do not insert power plug, as our normal supply is 230V/50Hz., which will damage the equipment.
3. Observe type of sockets of equipment power to avoid mechanical damage.
4. Do not forcefully place connectors to avoid the damage.
5. Strictly observe the instructions given by the Teacher/ Lab Instructor.

Instruction for Laboratory Teachers:-

1. Submission related to whatever lab work has been completed should be done during the next lab session.
2. Students should be instructed to switch on the power supply after getting the checked by the lab assistant / teacher. After the experiment is over, the students must hand over the circuit board, wires, CRO probe to the lab assistant/teacher.
3. The promptness of submission should be encouraged by way of marking and evaluation patterns that will benefit the sincere students.

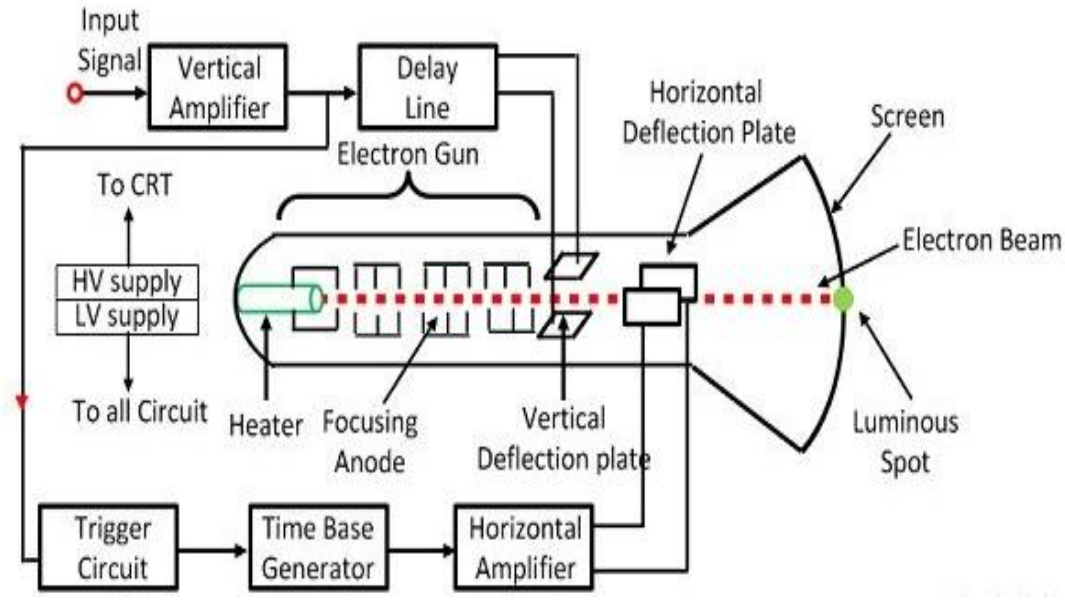
Pre requisite No. 1 :(2 Hours)

Aim: - To Study CRO and Function Generator.

Apparatus: CRO, Function Generator, Probes.

Theory:

Cathode Ray Oscilloscope (CRO)



The Oscilloscope is probably the single most versatile and useful Test and Measurement instrument invented for Electronic measurement applications. It is a complex instrument capable of measuring or displaying a variety of signals. This is the basic equipment used in almost all electronic circuit design and testing applications. CRO, Oscilloscope and Scope are the common names by which it is known. The major subsystems in a CRO are Power supplies (high and low voltage supplies), Display subsystem, Vertical deflection subsystem, and Horizontal deflection subsystem.

The main use of a CRO is to obtain the visual display of an electrical voltage signal. If the signal to be displayed is not in the voltage form, it is first converted to this form. The signal voltage is then transmitted to the oscilloscope along a cable

(usually a coaxial cable) and enters the oscilloscope where the cable is connected to the scope input terminals. Often the signal at this point is too small in amplitude to activate the scope display system (the Cathode Ray Tube or CRT). Therefore, it needs to be amplified. The function of the vertical deflection system is to perform such amplification. After suitable amplification, the input signal is applied to the vertical deflection plates of the scope CRT. Within the CRT, an electron beam is created by an electron gun. The electron beam is focused and directed to strike the fluorescent screen, creating a spot of light, where impact is made with the screen. The beam is deflected vertically in proportion to the amplitude of the voltage applied to the CRT vertical deflection plates. The amplified input signal is also monitored by the horizontal deflection system. This subsystem has the task of sweeping the electron beam horizontally across the screen at a uniform rate. A sawtooth type signal (a triangular/ramp signal with long time duration for the rising part of the ramp and very small time duration for the falling part) is internally generated in a CRO as a time-base signal (sweep signal). This signal is amplified and applied to the horizontal deflection plates of the CRO. Again, the beam is deflected horizontally in proportion to the amplitude of the voltage applied to the CRT horizontal deflection plates. The simultaneous deflection of the electron beam in the vertical direction (by the vertical deflection system and the vertical deflection plates) and in the horizontal direction (by the time-base circuitry and the horizontal deflection plates) causes the spot of light produced by the electron beam to trace a path across the CRT screen. For example, if the input signal to the CRO were a sine wave, the trace produced on the CRT screen will be a sine wave. It is important to obtain a stable display on the CRT screen. If the input signal is periodic and the time base circuitry properly synchronizes the horizontal sweep with the vertical deflection, the spot of light will trace the same path on the screen over and over again. For a periodic signal the input signal can be synchronized with the time-base signal using the Trigger controls and the time base controls. If the frequency of the periodic signal is high enough (say greater than 40 Hz), the repeating trace will appear to be a steady pattern painted by solid lines of light on the screen

Function Generator

Another major equipment, which is used commonly in electronic circuit applications, is a Function Generator (FG). As the name indicates, a Function Generator generates different voltage signals, such as Sine, Pulse, Triangle. The most commonly required signals in electronic circuits are Sine and Pulse. Sine wave signals find their use mostly in Analog circuits, such as amplifiers, filters, etc. Pulse signals are useful in testing the time response of circuits and also as Clock signals in Digital circuits. In a general pulse signal, the high and low level time periods are different. Square wave is a special case when the periods are equal.

In a FG by the touch of a button one can switch over from one signal to another one. This is possible because of the fact that one can obtain different signals from a starting signal using Wave shaping circuits. Most FGs generate a Triangular signal and derive Sine and Pulse signals from it.

<u>Conclusion</u>:-

Pre requisite No. 2 :(2 Hours)

Aim: - To Study Power Supply and Digital Multimeter.

Apparatus: CRO, Function Generator, Probes.

Theory:

Power Supply

Power Supply is designed as a Constant Current (CC) and Constant Voltage (CV) source for use in laboratories, industries and field testing. With compact size, light weight and low power loss it, provides DC output voltages for Analog and Digital testing. The DC output can be adjustable from 0 - 30 V with Coarse and Fine controls. Current limit is adjustable from 0 - 1A. Over loading is indicated by LED. A 3-digit LED display for voltage & current is used to read the values. These two parameters can be switched to display either voltage or current.

Properties

1. Output constant current adjustable.

2. Output constant voltage adjustable.

3. LCD voltage and current display.

4. Constant voltage and current operation in individual.

5. Over current protection.

Digital Multimeter

Types of Multimeters

There are two common types of Multimeters, Analog and Digital. Digital Multimeters (DMMs) are the most common. They use a liquid crystal display (LCD) technology to give more accurate readings. Other advantages include higher input impedances, which will not load down sensitive circuits, and input protection. Analog meters use a needle movement and calibrated scale to indicate values. These were popular for years, but recently their numbers have declined. Every voltmeter has an internal resistance or impedance. The input impedance of an analog meter is expressed in ―Ohms per Volt.

The Digital Multimeter (DMMs) feature a digital or liquid crystal display (LCD). Measurement readings are displayed as numerical values on the LCD Display.

Setting the Function The dial of the DMM allows you to choose the function you're interested in measuring. Whether you intend to measure one of the three elements of Ohm's Law, or a more advanced function like frequency or capacitance, you must first set the dial to the appropriate function. Setting the Range The dial also plays another essential role in measuring electricity – that of determining the range of measurement. The range you select on the dial determines the placement of the decimal point as it appears on the LCD. In turn, the position of the decimal point determines how refined, or precise, your reading is. This is called resolution.

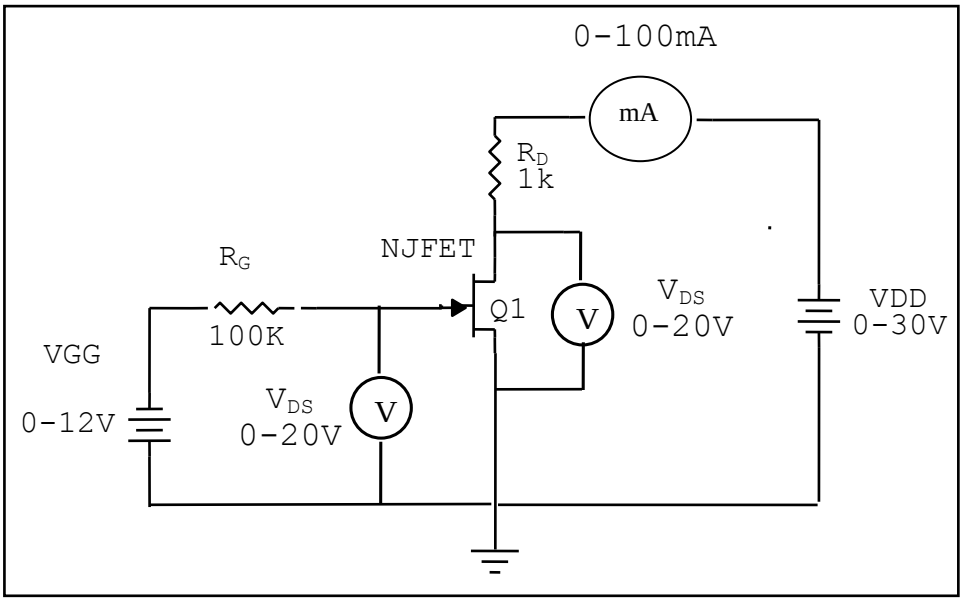
Conclusion:

Exercise No. 1 :(2 Hours)

Aim: - To plots the drain characteristics of N-channel JFET.

Apparatus: - JFET (BFW10), Regulated Power Supply (0-12V), Regulated Power Supply (0-30V), 02 Voltmeters (0-20V), Ammeter (0-100mA), Resistors, Bread board, connecting wires.

Circuit Diagram :-

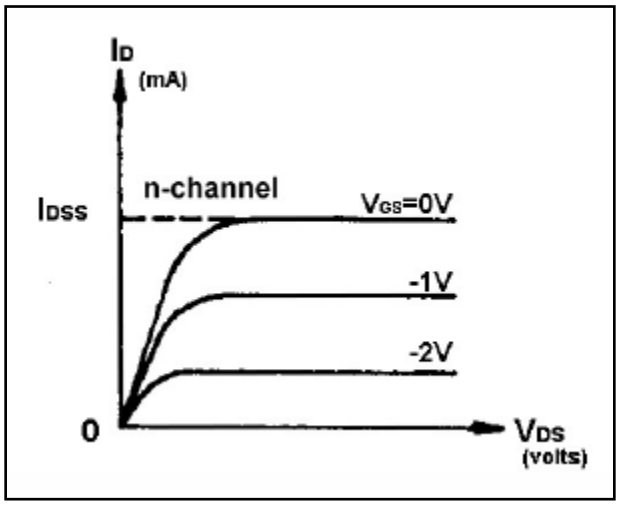


Theory:-

When V_{GS} = 0V, the voltage drop will be generated by V_{DD} , a current flows through the n-channel viewed as a small resistor, wherein the potential close to the drain-gate junction is higher than of source-gate junction. The reverse bias applied to P-N junction will thus form the depletion region. When the voltage source V_{DD} is increased, the current I_D will also be increased correspondingly, which will form the even larger depletion region and will generate the larger resistance between drain and source.

If the voltage source V_{DD} is continuously increased, the depletion region will eventually occupy the full channel. At this time any further increment of V_{DD} will

not increase I_D any more (I = V/R, V increases, R increases, I keeps constant). When V_{GS} = 0, the relation between V_{DS} and I_D is shown in Figure. From this figure we can clearly view that I_D will be increased with V_{DS} until it maintains at a constant value. This constant value is called Drain Saturation Current I_{DSS}.



If V_{GS} is increased (it's more negative to n-channel), depletion will be immediately generated in the channel so that the current required to pinch off the channel will be decreased. The curve corresponding to V_{GS} = -1V is also shown in Figure. From this result we can find out that the gate voltage functions as a controller capable of decreasing the drain current (at a specific voltage V_{DS}). If V_{GS} is more positive for p-channel JFET, the drain current will be decreased from I_{DSS}. If V_{GS} is continuously increased in reverse, the drain current will be decreased correspondingly. When V_{GS} reaches a certain value, the drain current will be decreased to zero and will be independent of the value of V_{DS}. The gate-source voltage at this time is called pinch-off voltage which is usually denoted as V_P or $V_{GS\ (off)}$. From Figure we can find out that V_P is a negative voltage for n-channel FET and a positive voltage for p-channel FET.

Procedure:-

Output characteristics:

1. Connect the milliammeter & voltmeters at the respective places.
2. Keep the V_{GG} & V_{DD} at minimum positions.
3. Switch on the power supply.
4. Keep the V_{GS} at fixed value say V_{GS}=0V
5. Now increase the V_{DD} in steps & note down the readings of I_D &V_{DS} with the 1V interval of V_{GS}
6. Plot the graph with V_{DS} along x axis & I_D along y axis.
7. Repeat the steps from 4 to 6 for different values of V_{GS}

Observations:-

Sr. No	V_{GS} = 0		V_{GS} = -1V		V_{GS} = -2V		V_{GS} = -3V	
	V_{DS}(V)	I_D(mA)	V_{DS} (V)	I_D(mA)	V_{DS} (V)	I_D(mA)	V_{DS} (V)	I_D(mA)
1	0.5		0.5		0.5		0.5	
2	1.0		1.0		1.0		1.0	
3	1.5		1.5		1.5		1.5	
4	2.0		2.0		2.0		2.0	
5	2.5		2.5		2.5		2.5	
6	3.0		3.0		3.0		3.0	
7	4.0		4.0		4.0		4.0	
8	5.0		5.0		5.0		5.0	
9	6.0		6.0		6.0		6.0	
10	7.0		7.0		7.0		7.0	
11	8.0		8.0		8.0		8.0	

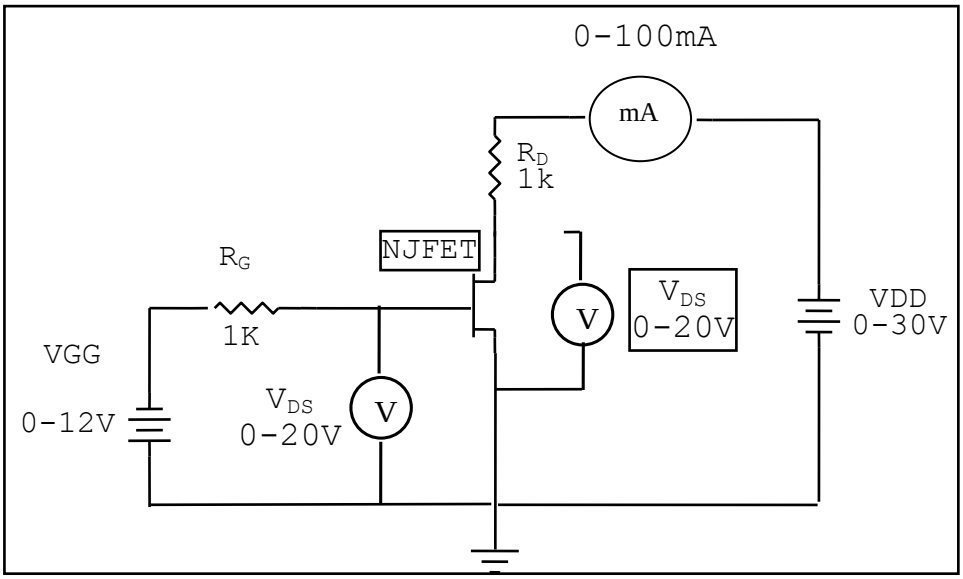
Conclusion: The drain characteristics of a JFET are drawn. The Drain saturation current I_{DSS} = _____

Exercise No. 2 :(2 Hours)

Aim: - **To** plot the drain characteristics of N-channel EMOSFET.

Apparatus: - EMOSFET (IRF840), Regulated Power Supply (0-12V), Regulated Power Supply (0-30V), 02 Voltmeters (0-20V), Ammeter (0-100mA), Resistors, Bread board, connecting wires.

Circuit Diagram :-

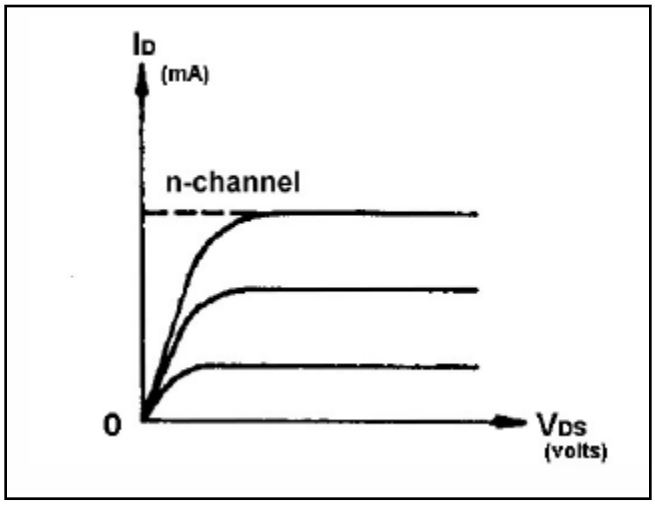


Theory:-

As its name indicates, this MOSFET operates only in the *enhancement mode* and has no depletion mode. It operates with large positive gate voltage only. It does not conduct when the gate-source voltage $V_{GS} = 0$. This is the reason that it is called normally-off MOSFET. In these MOSFET's drain current I_D flows only when V_{GS} exceeds V_{GST} [gate-to-source threshold voltage].

The minimum value of gate-to-source voltage V_{GS} that is required to form the inversion layer (N-type) is termed the *gate-to-source threshold voltage* V_{GST}. For V_{GS} below V_{GST}, the drain current $I_D = 0$. But for V_{GS} exceeding V_{GST} an N-type inversion layer connects the source to drain and the drain current I_D is large. Depending upon the device being used, V_{GST} may vary from less than 1 V to more

than 5 V.



Drain characteristics of an N-channel E-MOSFET are shown in figure. The lowest curve is the V_{GST} curve. When V_{GS} is lesser than V_{GST}, I_D is approximately zero. When V_{GS} is greater than V_{GST}, the device turns- on and the drain current I_D is controlled by the gate voltage. The characteristic curves have almost vertical and almost horizontal parts. The almost vertical components of the curves correspond to the ohmic region, and the horizontal components correspond to the constant current region. Thus E-MOSFET can be operated in either of these regions *i.e.* it can be used as a variable-voltage resistor (WR) or as a constant current source.

Procedure:-

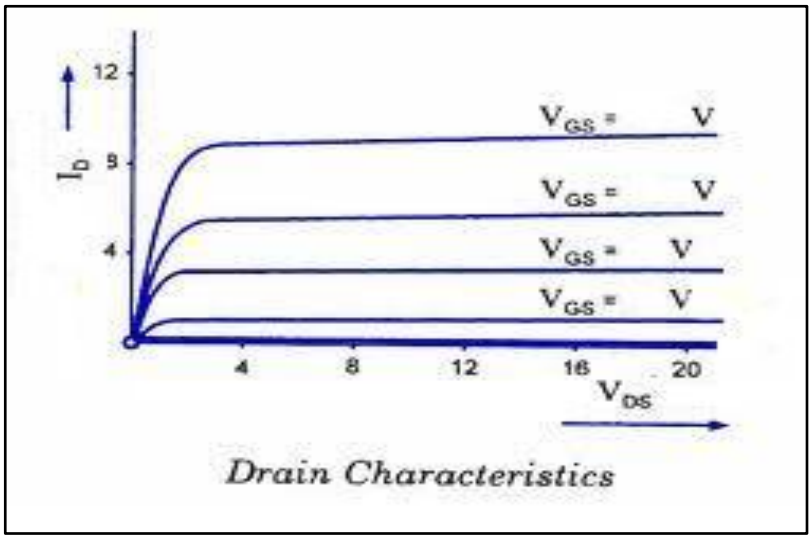
Output characteristics:

1. Connect the milliammeter & voltmeters at the respective places.
2. Keep the V_{GG} & V_{DD} at minimum positions.
3. Switch on the power supply.
4. Keep the V_{GS} at fixed value say V_{GS}=3V
5. Now increase the V_{DD} in steps & note down the readings of I_D &V_{DS} with the 1V interval of V_{GS}
6. Plot the graph with V_{DS} along x axis & I_D along y axis.
7. Repeat the steps from 4 to 6 for different values of V_{GS}

Observations:-

Sr.No	V_{GS} = 4V		V_{GS} = 5V		V_{GS} = 6V	
	V_{DS}(V)	I_D(mA)	V_{DS} (V)	I_D(mA)	V_{DS} (V)	I_D(mA)
1	0.1		0.1		0.1	
2	0.2		0.2		0.2	
3	0.3		0.3		0.3	
4	0.4		0.4		0.4	
5	0.5		0.5		0.5	
6	0.8		0.8		0.8	
7	1.0		1.0		1.0	
8	2.0		2.0		2.0	
9	3.0		3.0		3.0	
10	4.0		4.0		4.0	
11	5.0		5.0		5.0	

Drain Characteristics of MOSFET:



Drain Characteristics

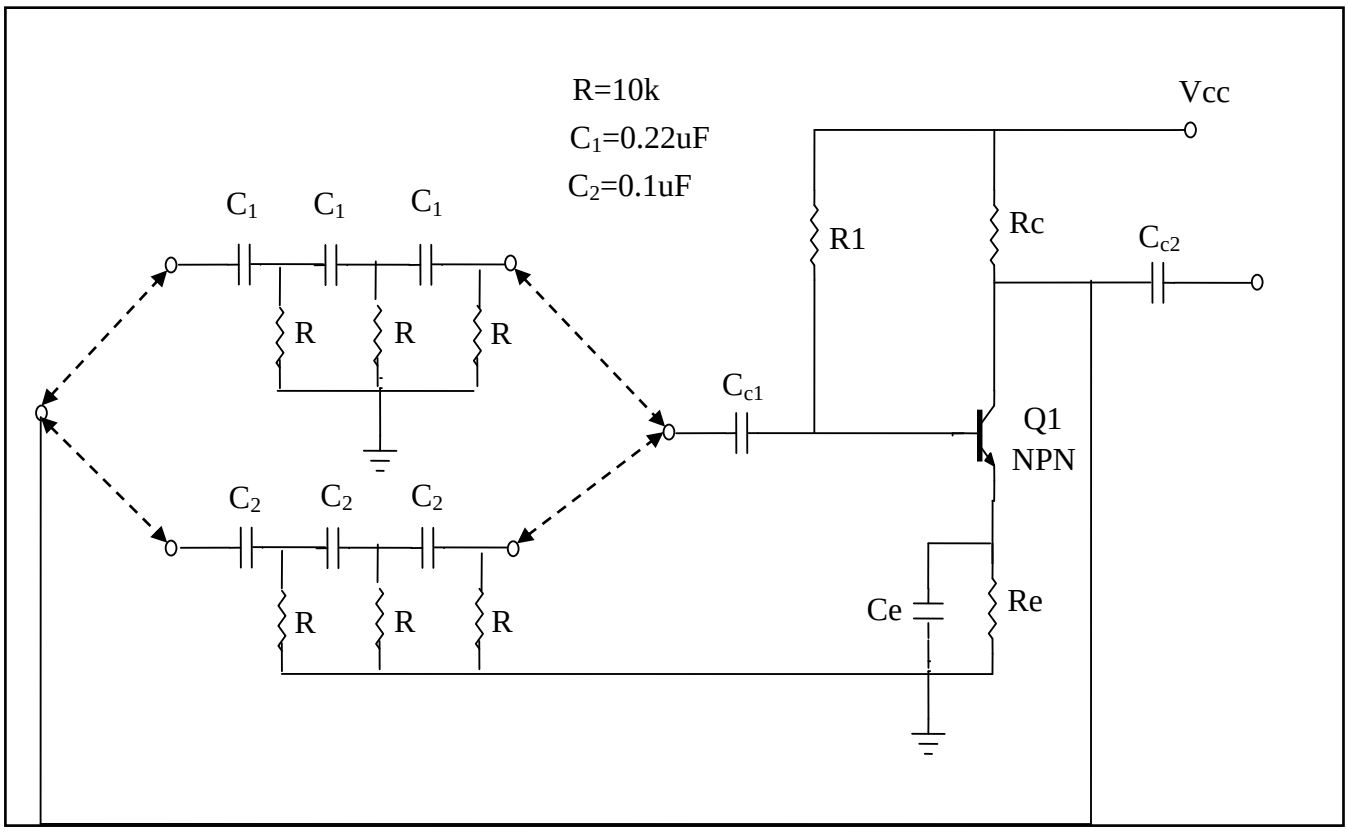
Conclusion:

Exercise No. 3:(2 Hours)

Aim: - To study the circuit of RC Phase shift Oscillator & Determine the frequency of Oscillator.

Apparatus: - RC Phase shift oscillator trainer kit, CRO, Probes, connecting wires.

Circuit Diagram :-



Theory:-

Oscillators generate periodic signals in the time domain. They convert DC power into AC signal power. Signal generation implies production of self-sustained oscillations. The most simple RC phase-shift oscillator configuration uses three buffered RC cells and a voltage amplifier with very high input impedance and very low output impedance.

The BJT RC Phase-Shift Oscillator is a popular configuration for the generation of low-frequency sine waves, starting at a few Hertz and up to about 100 kHz. A schematic diagram of a basic implementation can be seen in Fig.3. If the RC cells were isolated from each other, the phase shift per cell would be 60º. However, not being it the case, we need to perform a detailed analysis considering loading effects.

Procedure:-

1. Study the circuit provided on the front panel of the kit.
2. Connect CRO at O/P V_o terminal.
3. Now switch ON the power supply note different voltages as per observation table.
4. Observe & note the frequency of oscillation & amplitude on CRO.
5. Calculate the theoretical frequency of oscillation using formula.
6. Compare theoretical & practical frequency of oscillation.
7. Change RC network & repeat above procedure.

Equation:-

$$fo = \frac{1}{2\pi RC\sqrt{6N}}$$ (Where N= No of RC networks)

As N=3 $$fo = \frac{0.065}{RC}$$

Observations:-

1) With network 1 observed frequency of oscillation F_O = ------KHz
2) With network 2 observed frequency of oscillation F_O = ------KHz

Result:- 1) With network 1 frequency of oscillations is ---------- Hz(Calculated) and ----- Hz(Observed)

2) With network 2 frequency of oscillations is ---------- Hz(Calculated) and ----- Hz(Observed)

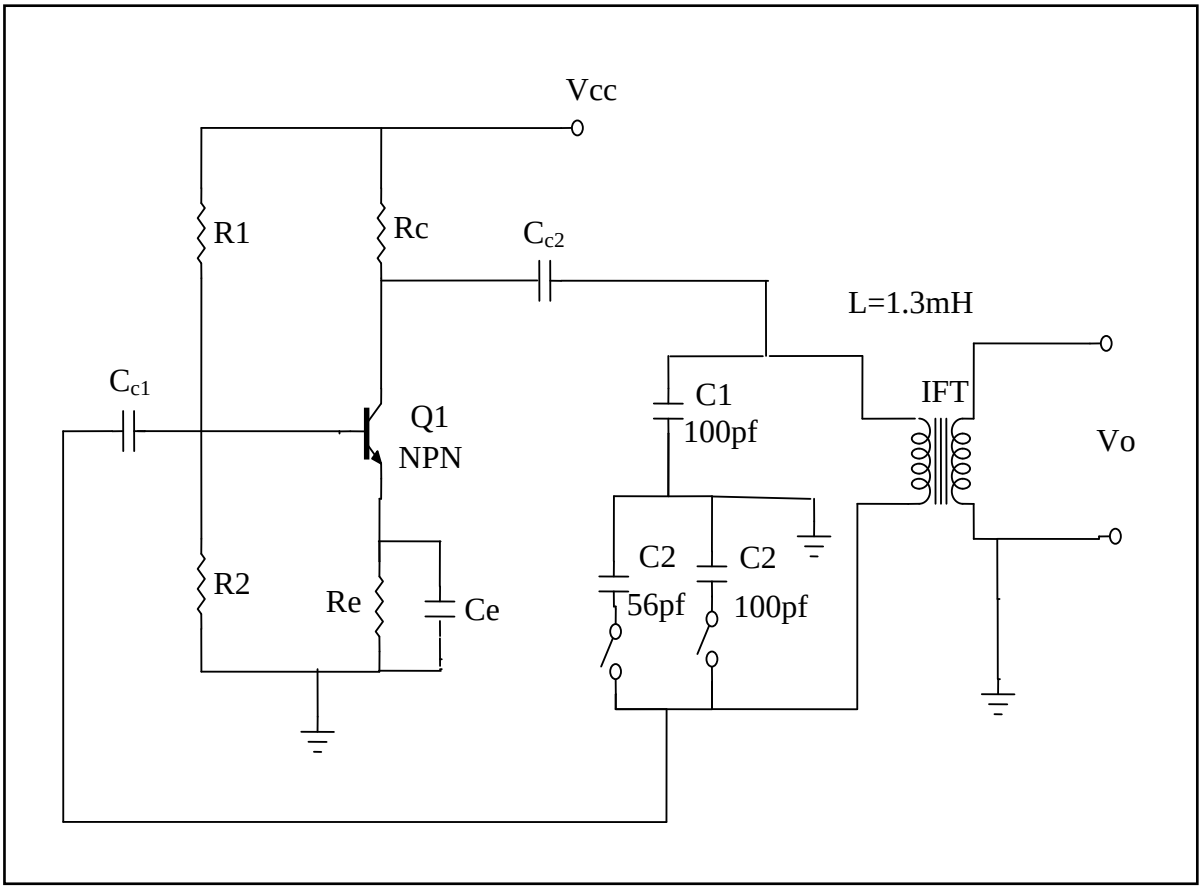
Conclusion:-

Exercise No. 4 :(2 Hours)

Aim: - To study the circuit of Colpitts or LC Oscillator & Determine the frequency of Oscillator.

Apparatus: - Colpitts oscillator trainer kit, CRO, Probes, connecting wires.

Circuit Diagram:-

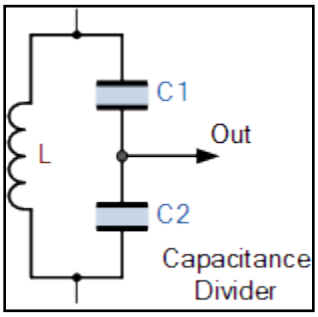


Theory:-

Oscillators generate periodic signals in the time domain. They convert DC power into AC signal power. Signal generation implies production of self-sustained oscillations.

In many ways, the Colpitts oscillator is the exact opposite of the Hartley

Oscillator we looked at in the previous tutorial. Just like the Hartley oscillator, the tuned tank circuit consists of an LC resonance sub-circuit connected between the collector and the base of a single stage transistor amplifier producing a sinusoidal output waveform.



Colpitts OscillatorTank Circuit

The Colpitts oscillator uses a capacitive voltage divider network as its feedback source. The two capacitors, C1 and C2 are placed across a single common inductor, L as shown. Then C1, C2 and Lform the tuned tank circuit with the condition for oscillations being: $X_{C1} + X_{C2} = X_L$, the same as for the Hartley oscillator circuit. The advantage of this type of capacitive circuit configuration is that with less self and mutual inductance within the tank circuit, frequency stability of the oscillator is improved along with a more simple design.

The configuration of the transistor amplifier is of a *Common Emitter Amplifier* with the output signal 180^o out of phase with regards to the input signal. The additional 180^ophase shift require for oscillation is achieved by the fact that the two capacitors are connected together in series but in parallel with the inductive coil resulting in overall phase shift of the circuit being zero or 360^o.

The amount of feedback depends on the values of C1 and C2. We can see that the voltage across C1 is the the same as the oscillators output voltage, Vout and that the voltage across C2 is the oscillators feedback voltage. Then the voltage across C1 will be much greater than that across C2. Therefore, by changing the values of capacitors, C1 and C2 we can adjust the amount of feedback voltage returned to the tank circuit. However, large amounts of feedback may cause the output sine wave to become distorted, while small amounts of feedback may not allow the circuit to oscillate.

Procedure:-

1. Study the circuit provided on the front panel of the kit.
2. Connect CRO at O/P V_o terminal.
3. Now switch ON the power supply note different voltages as per observation table.
4. Observe & note the frequency of oscillation & amplitude on CRO.
5. Calculate the theoretical frequency of oscillation using formula.
6. Compare theoretical & practical frequency of oscillation.
7. Change the values of capacitor C_2 & repeat above procedure.

Equation:-

$$fo = \frac{1}{2\pi\sqrt{LCeq}}$$

Where, $Ceq = \frac{C1.C2}{C1+C2}$

Observations:-

1) With C_2=56pf, observed frequency of oscillation F_O = ------KHz
2) With C_2=100pf, observed frequency of oscillation F_O = ------KHz

Result:- 1) With C_2=56pf, frequency of oscillations is ---------- Hz(Calculated) and ----- Hz(Observed)
2) With C_2=100pf, frequency of oscillations is ---------- Hz (Calculated) and ----- Hz (Observed)

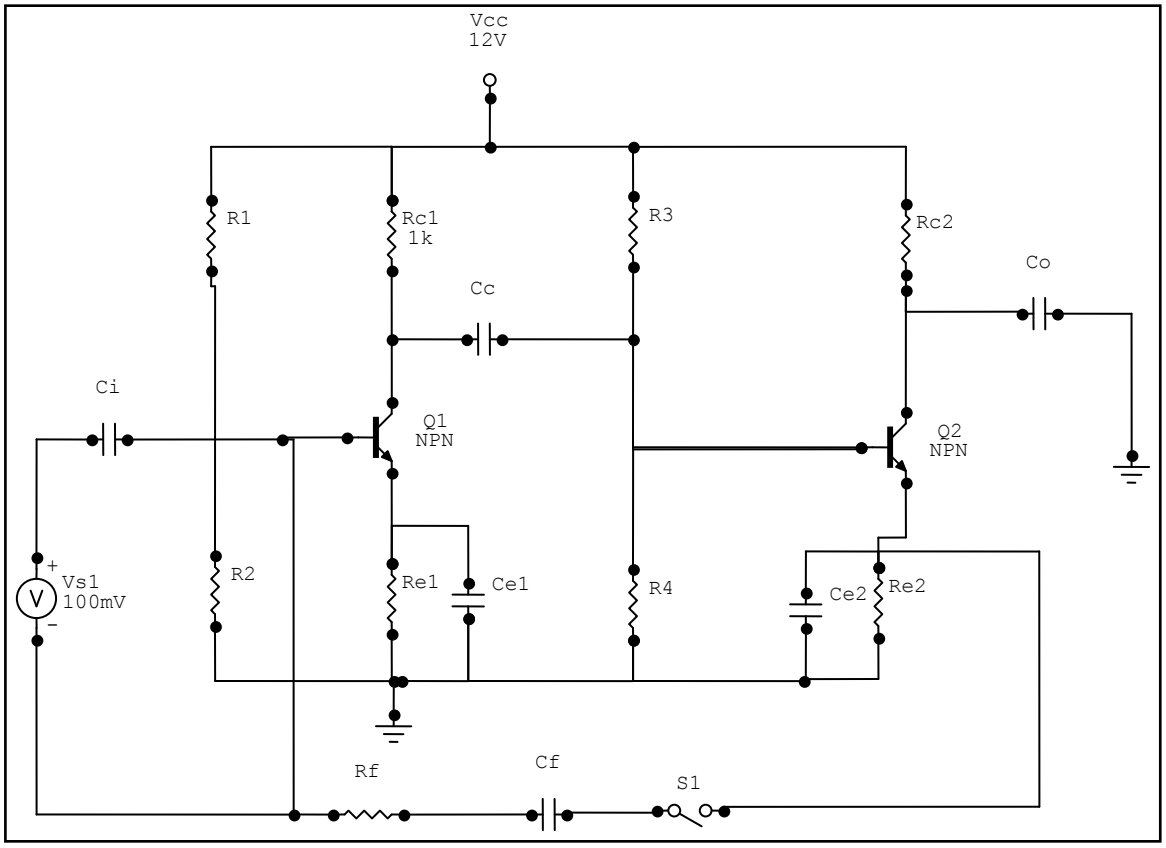
Conclusion:- The tank circuit from by center tap capacitor C_1 , C_2 & inductor L provides feedback to transistor amplifier which produces a sine wave O/P in RF so Colpitts Oscillator is also called as RF Oscillator.

Exercise No. 5 :(2 Hours)

Aim: - To study a two stage RC Coupled Amplifier with negative feedback using transistor and plot the frequency response to calculate the bandwidth.

Apparatus: -Amplifier trainer kit, Function Generator, CRO, Probes.

Circuit Diagram:-

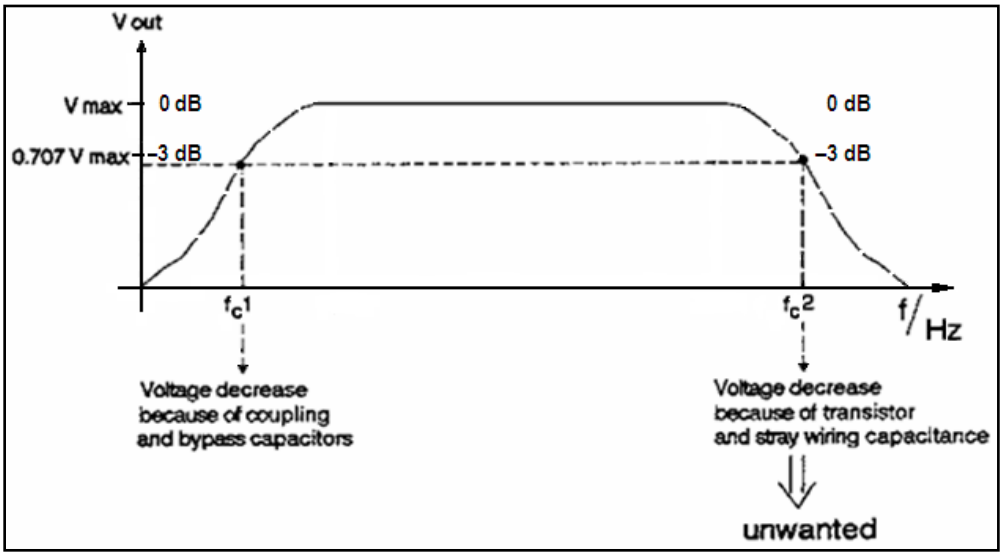


Theory:-

Practically the gain of a single stage amplifier is not sufficient for a particular application. The gain of an amplifier is increased by connecting the amplifiers in cascaded manner. The output of one stage is connected to the input of next stage through the coupling capacitor. It increases the overall gain of the amplifier and decreases the overall bandwidth of the amplifier. The two resistors

R1 andR2 are identical. The overall output is 360 phase shift. Hence output signal is in-phase with the input signal.

Frequency Response Curve



Then we can see that the frequency response of any given circuit is the variation in its behaviour with changes in the input signal frequency as it shows the band of frequencies over which the output (and the gain) remains fairly constant. The range of frequencies either big or small between f_L and f_H is called the circuit's bandwidth. So from this we are able to determine at a glance the voltage gain (in dB) for any sinusoidal input within a given frequency range.

Procedure:-

1) Connect the function generator at the input terminals of the circuit.
2) Connect the CRO at the output.
3) Switch on the power supply.
4) Keep the input signal amplitude V_i constant at 100 mV, so that transistors should not enter in saturation. Now vary the input frequency F_i from 20 Hz to 1MHz in steps. Observe & note the corresponding output voltage V_o. Find out the voltage gain $A_{v.}$
5) Plot the graph between input frequency & voltage gain and find the bandwidth.

Observations:-

Sr.No	Input Voltage Vi	Without Feedback		
		Frequency (Hz)	Output Voltage Vo (V)	Gain $Av = \frac{Vo}{0.1}$
1	100 mV (0.1V)	20		
2		50		
3		80		
4		100		
5		200		
6		500		
7		800		
8		1k		
9		2k		
10		5k		
11		8k		
12		10k		
13		20k		
14		50k		
15		80k		
16		100k		
17		200k		
18		500k		
19		1M		

Result:- With negative feedback, Av = ---------- , and Bandwidth = ---------- kHz

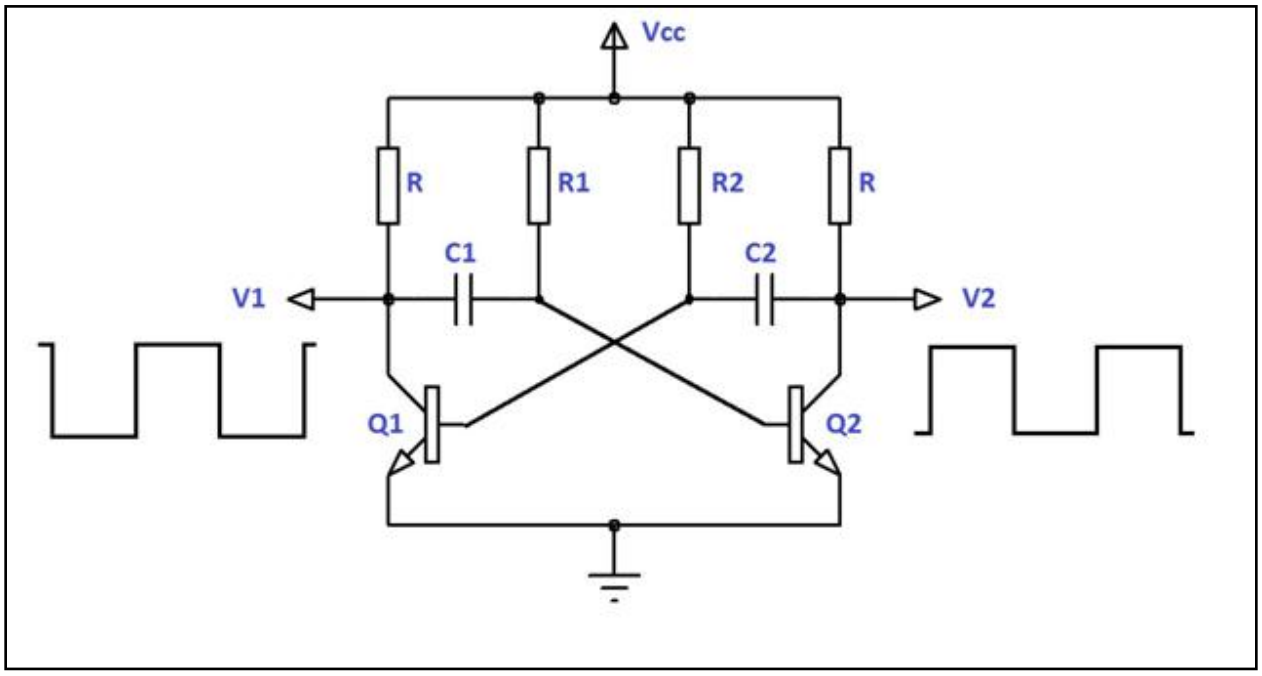
Conclusion:-

Exercise No. 6 :(2 Hours)

Aim: - To study a transistorized astable multivibrator circuit and calculate the frequency of oscillations and duty cycle of output waveform.

Apparatus: - Power Supply, CRO, Probes, Breadboard, Transistors, Resisters, Capacitors, Connecting Wires.

Circuit Diagram:-



Theory:-

Multivibrators

Individual Sequential Logic circuits can be used to build more complex circuits such as Counters, Shift Registers, Latches or Memories etc, but for these types of circuits to operate in a "Sequential" way, they require the addition of a clock pulse or timing signal to cause them to change their state. Clock pulses are generally square shaped waves that are produced by a single pulse generator circuit such as a Multivibrator which oscillates between a "HIGH" and a "LOW" state and

generally has an even 50% duty cycle, that is it has a 50% "ON" time and a 50% "OFF" time. Sequential logic circuits that use the clock signal for synchronization may also change their state on either the rising or falling edge, or both of the actual clock signals. There are basically three types of pulse generation circuits depending on the number of stable states.

1) Astable - has NO stable states but switches continuously between two states this action produces a train of square wave pulses at a fixed frequency.

2) Monostable - has only ONE stable state and if triggered externally, it returns back to its first stable state.

3) Bistable - has TWO stable states that produce a single pulse either positive or negative in value.

Astable Multivibrators:

The astable circuit has no stable state. With no external signal applied, the transistors alternately switch from cutoff to saturation at a frequency determined by the RC time constants of the coupling circuits. Astable multivibrator circuit consists of two cross coupled RC amplifiers which has two amplifying devices cross-coupled by resistors and capacitors.

The circuit has two states

State 1: VC1 LOW, VC2 HIGH, Q1 ON (saturation) and Q2 OFF.

State 2: VC1 HIGH, VC2 LOW, Q1 OFF and Q2 ON (saturation).

It continuously oscillates from one state to the other.

Procedure:-

1. Connect the circuit components as per the circuit diagram.
2. Connect CRO at O/P V_o terminal.
3. Now switch ON the power supply note different voltages as per observation table.
4. Observe & note the frequency of oscillation & duty cycle on CRO.
5. Calculate the theoretical frequency of oscillation & duty cycle using formula.
6. Compare theoretical & practical values.

Equation:-

For $R_1 = R_2$ and $C_1 = C_2$

$$fo = \frac{1}{1.4RC}$$

And Duty Cycle = 50%

Observations:-

1) Frequency of oscillations, F_O = ------KHz
2) Duty Cycle, D = ------

Result:- 1) Frequency of oscillations, F_O = ------KHz (Calculated) and --------- KHz (Observed)
2) Duty Cycle, D = ------ (Calculated) and D = ----- KHz (Observed)

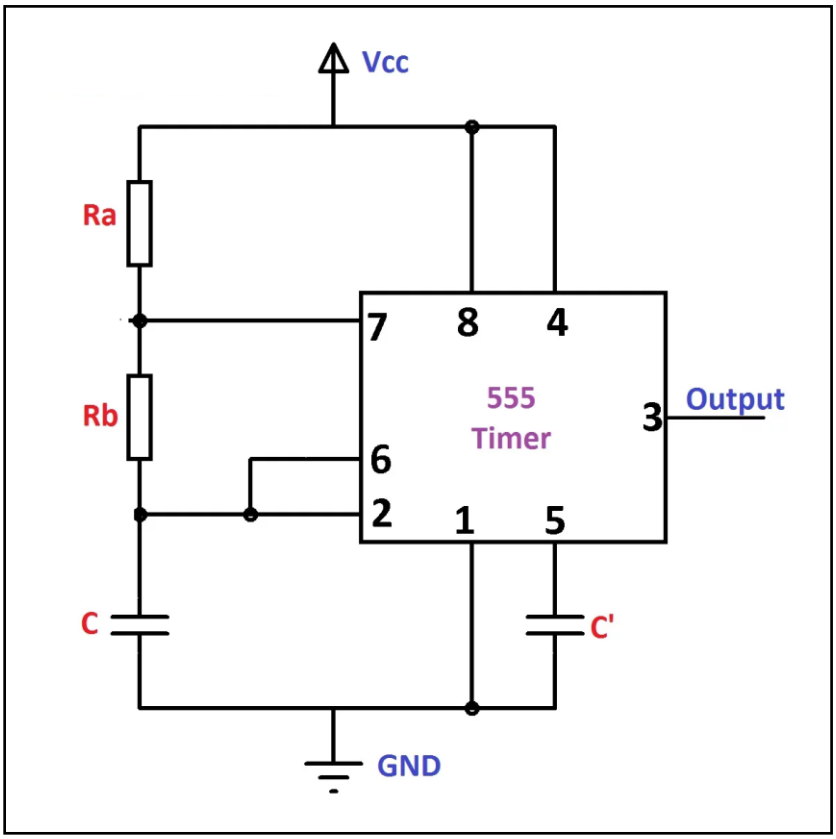
Conclusion:-

Exercise No. 7 :(2 Hours)

Aim: - To study an astable multivibrator circuit using IC 555 and calculate the frequency of oscillations and duty cycle of output waveform.

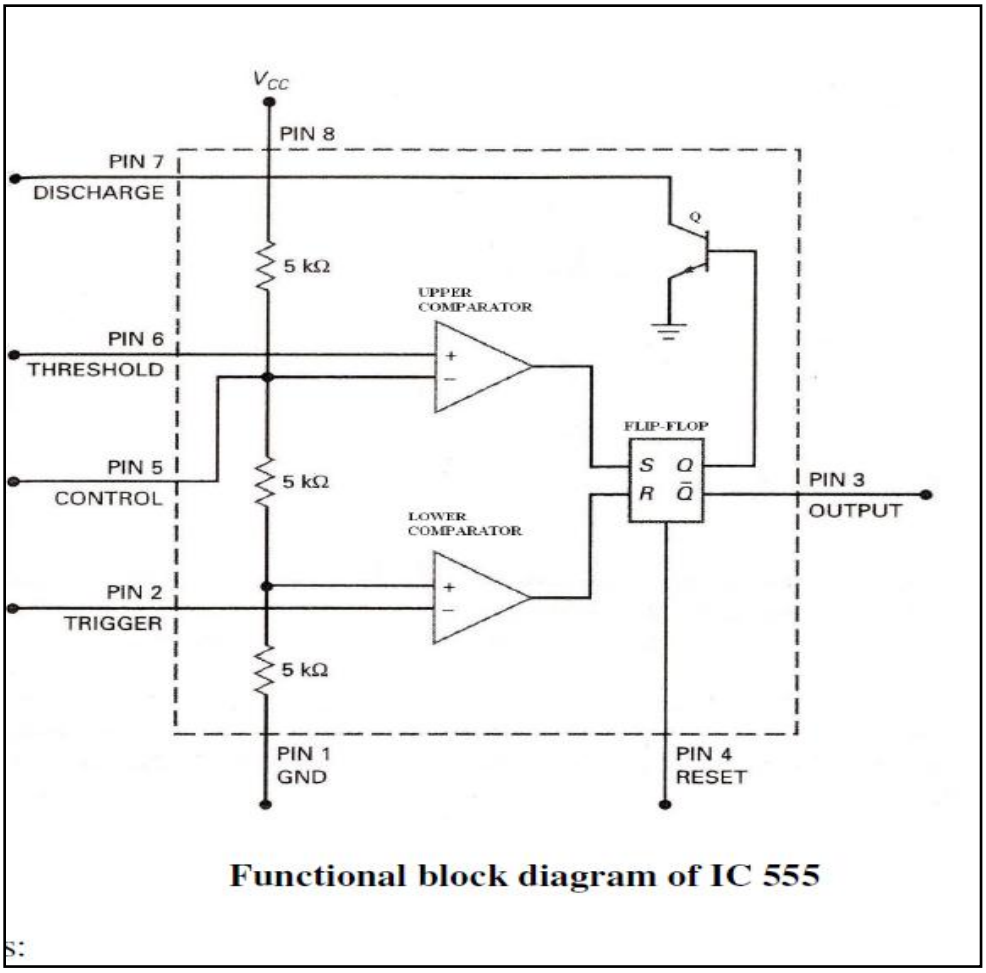
Apparatus: - Power Supply, CRO, Probes, Breadboard, IC555, Resisters, Capacitors, Connecting Wires.

Circuit Diagram:-



Theory:-

The **555 timer IC** is an integrated circuit (chip) used in a variety of timer, pulse generation, and oscillator applications. The 555 can be used to provide time delays, as an oscillator, and as a flip-flop element.



Functional block diagram of IC 555

S:

IC 555 Timer as Multivibrator

The 555 can operate in either monostable or astable mode, depending on the connections to and the arrangement of the external components. Thus, it can either produce a single pulse when triggered, or it can produce a continuous pulse train as longas it remains powered.

Astable multivibrator

These circuits are not stable in any state and switch outputs after predetermined time periods. The result of this is that the output is a continuous square/rectangular wave with the properties depending on values of external resistors and capacitors. Thus, while designing these circuits following parameters need to be determined:

1. Frequency (or the time period) of the wave.
2. The duty cycle of the wave.

The time for charging C from 1/3 to 2/3 Vcc, i.e, ON Time = 0.693 ($R_A + R_B$). C
The time for discharging C from 2/3 to 1/3 Vcc, i.e. OFF Time = 0.693 R_B. C
To get the total oscillation period, just add the two:

Tosc = 0.693(R_A+R_B)C + 0.693(R_B)C = 0.693(R_A + 2R_B)C

Thus,

fosc = 1/ Tosc = 1.44/(R_A + 2R_B).C

Duty cycle = (R_A+R_B)/(R_A + 2R_B)

Procedure:-

1. Connect the circuit components as per the circuit diagram.
2. Connect CRO at O/P V_o terminal.
3. Now switch ON the power supply note different voltages as per observation table.
4. Observe & note the frequency of oscillation & duty cycle on CRO.
5. Calculate the theoretical frequency of oscillation & duty cycle using formula.
6. Compare theoretical & practical values.

Equation:-

$$fo = \frac{1}{0.693(Ra+Rb)C}$$

$$D = \frac{Ra+Rb}{(Ra+2Rb)}$$

Observations:-

1) Frequency of oscillations, F_O = ------KHz
2) Duty Cycle, D = ------

Result:- 1) Frequency of oscillations, F_O = ------KHz (Calculated) and --------- KHz (Observed)

2) Duty Cycle, D = ------ (Calculated) and D = ----- KHz (Observed)

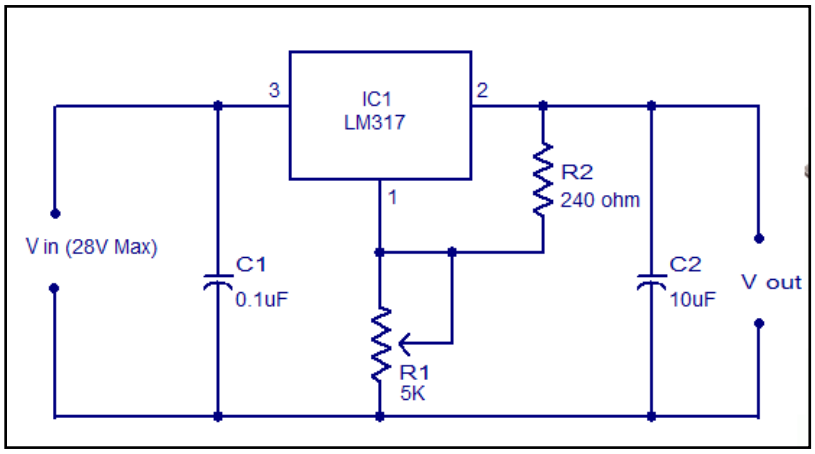
Conclusion:-

Exercise No. 8 :(2 Hours)

Aim: - To design an Adjustable Voltage Regulator using IC LM 317.

Apparatus: - Power Supply, Bread Board, IC 317, Resister, Potentiometer, Capacitors, Voltmeter & Connecting wires.

Circuit Diagram:-



Theory:-

Voltage regulator

The LM317 has three pins: INput, OUTput, and ADJustment. Internally the device has a bandgap voltage reference which produces a stable reference voltage of V_{ref}= 1.25 V followed by a feedback-stabilized amplifier with a relatively high output current capacity. How the adjustment pin is connected determines the output voltage as follows.

If the adjustment pin is connected to ground the output pin delivers a regulated voltage of 1.25 V at currents up to the maximum. Higher regulated voltages are obtained by connecting the adjustment pin to a resistive voltage divider between the output and ground. Then

$$V_{out} = V_{ref} (1 + R_L/R_P)$$

V_{ref} is the difference in voltage between the OUT pin and the ADJ pin. V_{ref} is typically 1.25 V during normal operation.

Because some quiescent current flows from the adjustment pin of the device, an error term is added:

$$V_{out} = V_{ref} (1 + R_L/R_H) + I_Q R_L$$

To make the output more stable, the device is designed to keep the quiescent current at or below 100µA, making it possible to ignore the error term in nearly all practical cases.

Procedure:-

1. Connect the circuit components as per the circuit diagram.
2. Connect Voltmeter at O/P V_o terminal.
3. Now switch ON the power supply and apply input voltage of 22V DC.
4. Observe & note the minimum and maximum value of output voltage by varying the potentiometer.

Observations:-

Input Voltage V_{IN}	**Output Voltage V_{OUT}**	
	Using potentiometer to ADJ pin	
	Minimum V_{OUT}	**Maximum V_{OUT}**

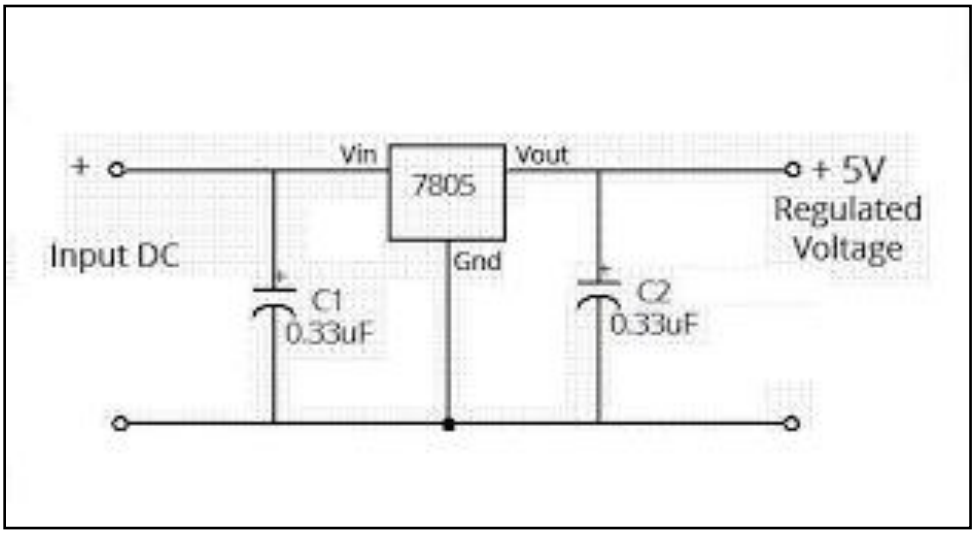
Conclusion:-

Post requisite No. 1 :(2 Hours)

Aim: - To design a +5V Voltage Regulator using IC 7805.

Apparatus: - Power Supply, Bread Board, IC 7805, IC 7905, Resister, Potentiometer, Capacitors, Voltmeter & Connecting wires.

Circuit Diagram:-



Theory:-

Fixed positive voltage regulator IC Family

78xx is a family of self-contained fixed linear voltage regulator integrated circuits. The 78xx family is commonly used in electronic circuits requiring a regulated power supply due to their ease-of-use and low cost:

IC7805:

IC 7805 is a 5V Voltage Regulator that restricts the output voltage to 5V output for various ranges of input voltage. It acts as an excellent component against input voltage fluctuations for circuits, and adds an additional safety to your circuitry. It is inexpensive, easily available and very much commonly used. With few capacitors and this IC you can build pretty solid and reliable voltage regulator in no time. A Circuit diagram with pinout is given. It also comes with provision to add heatsink.

The maximum value for input to the voltage regulator is 35V. It can provide a constant steady voltage flow of 5V for higher voltage input till the threshold limit of 35V. If the input voltage is near to 7.2V to 12V then it does not produce any heat and hence no need of heatsink. Higher the input volts - the more it gets heated up, and excess electricity is liberated as heat from 7805. Hence the provision of heatsink. IC7805 also comes as smaller SMD component as well.

IC 7805 is a series of 78XX voltage regulators. It's a standard, from the name the last two digits 05 denotes the amount of voltage that it regulates. Hence a 7805 would regulate 5v and 7806 would regulate 6V and so on.

There are 3 pins in IC 7805, pin 1 takes the input voltage and pin 3 produces the output voltage. The GND of both input and out are given to pin 2.

Procedure:-

1. Connect the circuit components as per the circuit diagram.
2. Connect Voltmeter at O/P V_o terminal.
3. Now switch ON the power supply and apply input voltage in steps from 1V DC to 12V DC.
4. Observe & note output voltage and plot the variations on graph paper.

Observations:-

Input Voltage V_{IN} (V)	Output Voltage V_{OUT}(V)
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	

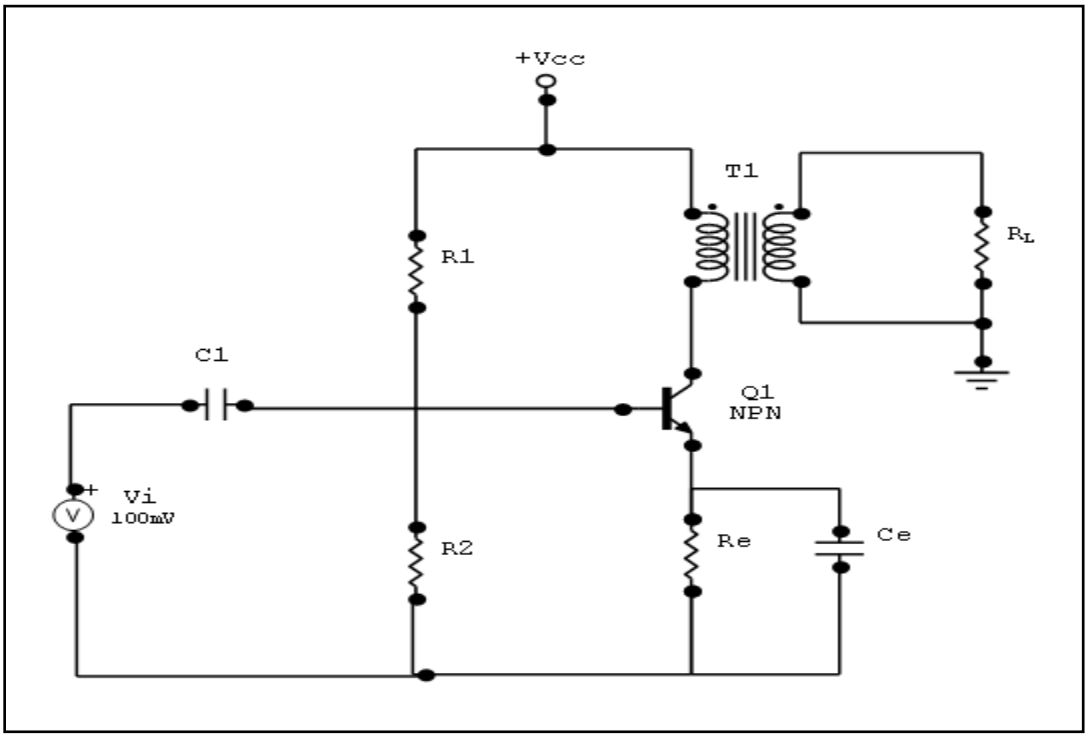
Conclusion:-

Post requisite No. 2 :(2 Hours)

Aim: - To study of class A transformer coupled amplifier and plot the frequency response.

Apparatus: -Amplifier trainer kit, Function Generator, CRO, Probes.

Circuit Diagram:-



Theory:-

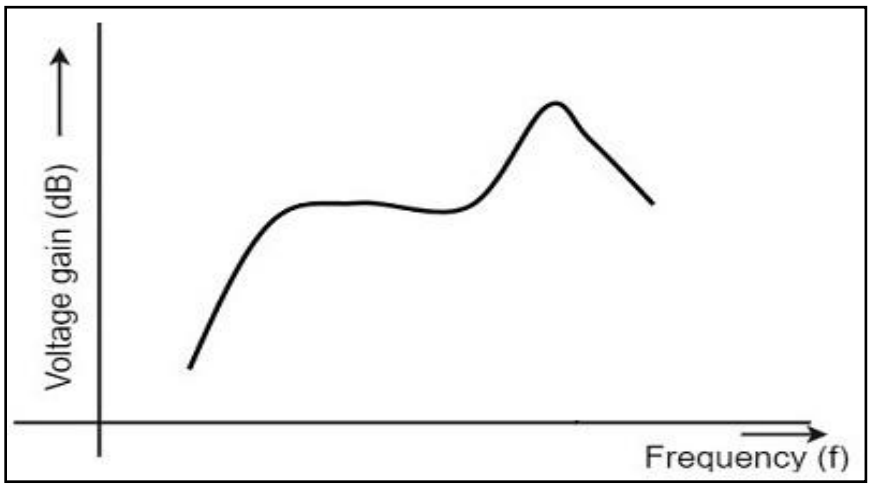
The most commonly used type of power amplifier configuration is the Class A Amplifier. The Class A amplifier is the simplest form of power amplifier that uses a single switching transistor in the standard common emitter circuit configuration as seen previously to produce an inverted output. The transistor is always biased "ON" so that it conducts during one complete cycle of the input signal waveform producing minimum distortion and maximum amplitude of the output signal.

The efficiency of this type of circuit is very low (less than 30%) and delivers

small power outputs for a large drain on the DC power supply. A Class A amplifier stage passes the same load current even when no input signal is applied so large heatsinks are needed for the output transistors.

To improve the full power efficiency of the Class A amplifier it is possible to design the circuit with a transformer connected directly in the Collector circuit to form a circuit called a Transformer Coupled Amplifier. The transformer improves the efficiency of the amplifier by matching the impedance of the load with that of the amplifiers output using the turns ratio (n) of the transformer.

Frequency Response Curve



Procedure:-

1) Connect the function generator at the input terminals of the circuit.
2) Connect the CRO at the output.
3) Switch on the power supply.
4) Keep the input signal amplitude V_i constant at 100 mV, so that transistors should not enter in saturation. Now vary the input frequency F_i from 20 Hz to 1MHz in steps. Observe & note the corresponding output voltage V_o. Find out the voltage gain $A_{v.}$
5) Plot the graph between input frequency & voltage gain and find the bandwidth.

Observations:-

Sr.No	Input Voltage Vi	Without Feedback		
		Frequency (Hz)	Output Voltage Vo (V)	Gain $Av = \frac{Vo}{0.5}$
1	100 mV (0.1V)	20		
2		50		
3		80		
4		100		
5		200		
6		500		
7		800		
8		1k		
9		2k		
10		5k		
11		8k		
12		10k		
13		20k		
14		50k		
15		80k		
16		100k		
17		200k		
18		500k		
19		1M		

Result:- Tuned frequency of amplifier, F_T = ----------

Conclusion:-

3.Quiz on the subject:-

1. An ideal power supply has
   a) zero internal resistance
   b) very high internal resistance
   c) high output resistance
   d) both (b) and (c)

2. A BJT is said to be operating in saturation region if
   a) both junctions are reverse biased
   b) both junctions are forward biased
   c) base emitter junction is forward biased and base collector junction is reverse biased
   d) base collector junction is forward biased and base emitter junction is reverse biased

3. An increase in ambient temperature means that maximum power rating of transistor
   a) will increase
   b) will decrease
   c) may increase or decrease
   d) may increase or remain the same

4. In a N-P-N transistor, when emitter junction is forward biased and collector junction is reverse biased, the transistor will operate in
   a) active region
   b) saturation region
   c) cut of region
   d) inverted region

5. The *h* parameter equivalent circuit of BJT has one voltage source and one current source.
   a) True
   b) False

6. The minimum gate source voltage that creates an inversion layer is called
   a) cut off voltage
   b) on voltage
   c) threshold voltage
   d) zener voltage

7. The most common method for biasing a JFET is
   a) gate bias
   b) self bias
   c) fixed bias
   d) voltage divider bias

8. At room temperature the current in an intrinsic semiconductor is due to
   a) holes
   b) electrons
   c) ions
   d) holes and electrons

9. The most commonly used semiconductor material is
   a) silicon
   b) germanium
   c) Carbon
   d) mixture of silicon and germanium

10. Which of the following is not a semiconductor
   a) silicon
   b) germanium
   c) Carbon
   d) Gallium

11. In which of these is reverse recovery time nearly zero?
   a) Zener diode
   b) Tunnel diode
   c) Schottky diode
   d) PIN diode

12. A transistor has a current gain of 0.99 in the CB mode. Its current gain in the CC mode is
    a) 100
    b) 99
    c) 1.01
    d) 0.99

13. In an *n* channel JFET, the gate is
    a) *n* type
    b) *p* type
    c) *either p or n* type
    d) Intrinsic

14. In an *n-p-n* transistor, the majority carriers in the base are
    a) electrons
    b) holes
    c) both holes and electrons
    d) either holes or electrons

15. The number of doped regions in PIN diode is
    a) 0
    b) 1
    c) 2
    d) 3

16. Recombination produces new electron-hole pairs
    a) True
    b) False

17. Crossover distortion behaviour is characteristic of
    a) class A O/P stage
    b) class B O/P stage
    c) class AB O/P stage
    d) class C O/P stage

18. In an *n-p-n* transistor biased for operation in forward active region
    a) emitter is positive with respect to base
    b) collector is positive with respect to base
    c) base is positive with respect to emitter and collector is positive with respect to base
    d) none of the above

19. A zener diode is used in
    a) voltage regulator circuit
    b) amplifier circuits
    c) both voltage regulator and amplifier circuit
    d) none of the above

20. In a bipolar transistor which current is largest
    a) emitter current
    b) base current
    c) collector current
    d) reverse leakage current

21. A *p-n* junction diode has
    a) low forward and high reverse resistance
    b) a non-linear *v-i* characteristics
    c) zero forward current till the forward voltage reaches cut in value
    d) all of the above

22. Which of the following is used for generating time varying wave forms?
    a) MOSFET
    b) PIN diode
    c) Tunnel diode
    d) UJT

23. The voltage across a zener diode
    a) is constant in forward direction
    b) is constant in reverse direction
    c) is constant in both forward and reverse direction

d) none of the above

24. When a *p*-*n* junction is forward biased
    a) the width of depletion layer increases
    b) the width of depletion layer decreases
    c) the majority carriers move away from the junction
    d) the current is very small

25. The depletion layer around *p*-*n* junction in JFET consists of
    a) holes
    b) electrons
    c) both holes and electron
    d) immobile charges

4. Conduction of Viva-Voce Examinations:

Teacher should conduct oral exams of the students with full preparation. Normally, the objective questions with guess are to be avoided. To make it meaningful, the questions should be such that depth of the students in the subject is tested. Oral examinations are to be conducted in cordial environment amongst the teachers taking the examination. Teachers taking such examinations should not have ill thoughts about each other and courtesies should be offered to each other in case of difference of opinion, which should be critically suppressed in front of the students.

5. Evaluation and marking system:

Basic honesty in the evaluation and marking system is absolutely essential and in the process impartial nature of the evaluator is required in the examination system to become. It is a primary responsibility of the teacher to see that right students who are really putting up lot of hard work with right kind of intelligence are correctly awarded.

The marking patterns should be justifiable to the students without any ambiguity and teacher should see that students are faced with just circumstances.