Mahatma Gandhi Mission

Jawaharlal Nehru Engineering College

Aurangabad, Maharashtra

Affiliated to Dr. B. A. Technological University, Lonere

NAAC 'A' Grade, ISO 9001:2015, 14001:2015 Certified, AICTE Approved.

Second Year B. Tech

Department of Information Technology

Lab Book

BTITL306 : Switching Theory and Logic Design Lab

Name: _____

Class:_____ Roll No: _____ Year: _____

Exam No.:_____

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Lab Book

BTITL306 : Switching Theory and Logic Design Lab

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Principal

Vision of Information Technology Department:

To develop expertise of budding technocrats by imparting technical knowledge and human value based education.

Mission of Information Technology Department:

A. Equipping the students with technical skills, soft skills and professional attitude.
B. Providing the state of art facilities to the students to excel as competent professionals, entrepreneurs and researchers.

Programme Educational Objectives:

PEO1. The graduates will utilize their **expertise** in IT industry and solve industry technological problems.
PEO2. Graduates should excel in **engineering positions** in industry and other organizations that emphasize design & implementation of IT applications.
PEO3. Graduates will be **innovators & professionals** in technology development, deployment & system implementation.
PEO4. Graduates will be pioneers in engineering, engineering management, research and **higher education**.
PEO5. Graduates will be good citizens & cultured human being with full appreciation of importance of IT **professional ethical & social** responsibilities.

Program specific outcomes

- PSO1. An ability to design, develop and implement computer programs in the areas related to Algorithms, Multimedia, Website Design, System Software, DBMS and Networking.
- PSO2. Develop software systems that would perform tasks related to Research, Education and Training and/or E governance.
- PSO3. Design, develop, test and maintain application software that would perform tasks related to information management and mobiles by utilizing new technologies to an individual or organizations.

Lab outcomes: After the completion of this course students will be able to,

LO1: 1.Understanding working and importance Basic Logic Gates and Boolean functions using Gates
LO2: Implementation of f code conversions half adder and Full adder

LO3: Implementation of Multiplexer, De multiplexer, flip flops and Decade Counter

Mandatory instructions for students:

1. Students should report to the concerned labs as per the given timetable.
2. Students should make an entry in the log book whenever they enter the labs during practical or for their own personal work.
3. When the experiment is completed, students should shut down the computers and make the counter entry in the logbook.
4. Any damage to the lab computers will be viewed seriously.
5. Students should not leave the lab without concerned faculty's permission.

Mahatma Gandhi Mission

Jawaharlal Nehru Engineering College

N-6, CIDCO Aurangabad – 431003

INDEX OF EXPERIMENTS

Sr. No.	Title of Experiment	Page No.	Date	Remark

This is to certify that Mr./Ms. _____of class S.Y. B.Tech Roll No._____has performed the experiments mentioned above in the premises of institution.

Date: **Lecturer in charge** **Head of Dept.** **Principal**

Experiment No.1

(A) **Study of basic logic Gates**

Aim: To Study basic logic gates such as AND, OR, NOT

Apparatus: Bread board, wires, IC-7402(AND), 7432(OR), 7404 (NOT)

Theory:

1. **AND**: Logical AND operation is defined as "**the output is 1 if all the inputs are 1"**

Circuit of logical AND is shown below. It has N inputs (N >= 2) and one output. Digital signals are applied at the input terminal marked A,B,C….,N ,the other terminal being grounded(not shown in diagram)The output is obtained at the terminal marked Y, and it is also a digital signal.

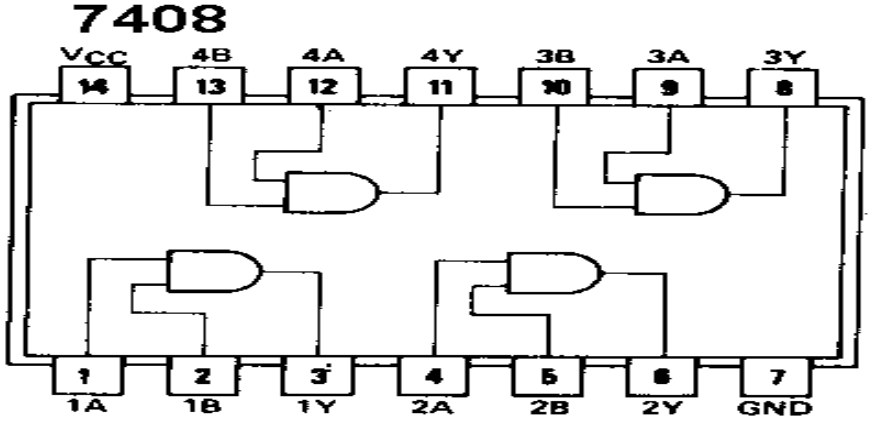


Fig1.1 LOGIC DIAGRAM OF AND GATE

Truth Table for AND operation

INPUTS		OUTPUTS
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Mathematically, **AND** operation is written as
Y=A **AND** B **AND** C
Y=A .B. C
Y=ABC…..N

2. OR: Logical **OR** operation is defined as "**the output is 1 if at least one of the inputs is 1".** Circuit of logical OR is shown below. It has N inputs (N>=2) and one output. Digital signals are applied at the input terminal marked A, B, C…., N, the other terminal being grounded (not shown in diagram).The output is obtained at the terminal marked Y, and it is also a digital signal.

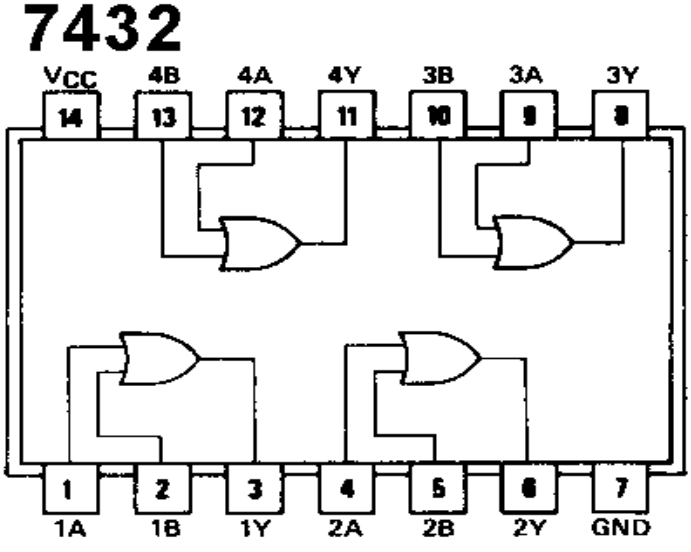


Fig 1.2 LOGIC DIAGRAM OF OR GATE

Mathematically,
OR operation is written as
Y=A OR B OR C
Y=A +B+C+……+N

Truth Table for **OR** operation

INPUTS		OUTPUTS
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

3. **NOT**: Logical NOT operation is also called as Inverter. It has one input (A) and one output (Y).Its logic Equation is written as
Y = NOT A
And is read as "Y equals not A" or "Y equals complement of A".

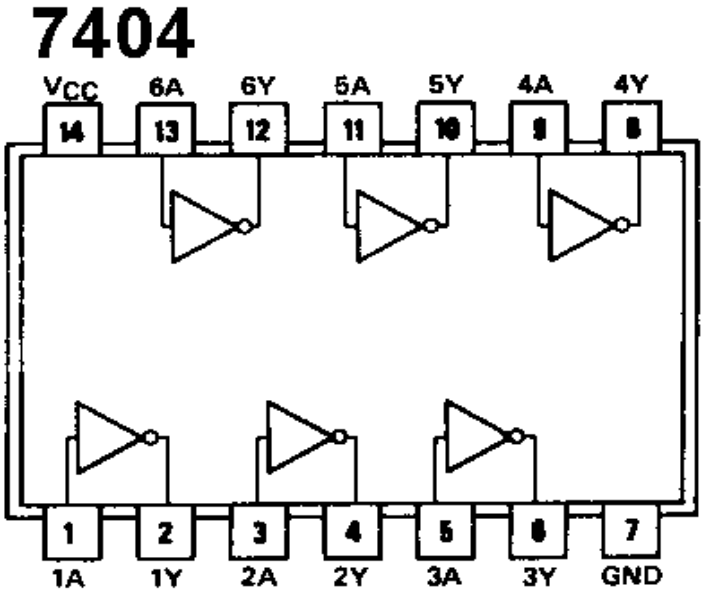


Fig 1.3 LOGIC DIAGRAM OF NOT GATE

Truth Table for N**OT** operation

INPUT	OUTPUT
A	Y
0	1
1	0

Procedure: -1) Apply Vcc to pin number 14 of all IC's & ground to pin number 7.

2) Assemble the circuit on breadboard according to the pin configuration.

3) Give the logical inputs and check for the proper output.

Conclusion: Hence verified the logical **AND, OR, NOT** Operation.

(B) **Study of Universal Gates**
Aim: To Study Universal gates such as NAND, NOR and Special gate X-OR
Apparatus: Bread board, wires, IC-740O (NAND), 7402 (NOR), 7486 (NOT)

Theory:

1. N**AND**: Combination of NOT and AND gate is called NAND gate It is a Reverse operation of AND gate.

Logical NAND operation is defined as "Its output only be at "0" when

All **its** inputs are also at "1" otherwise its output will be "1".

Logical equation of NAND

Y = complement (A. B)

Logic symbol of NAND Gate

Truth Table for NAND operation

INPUTS		OUTPUTS
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

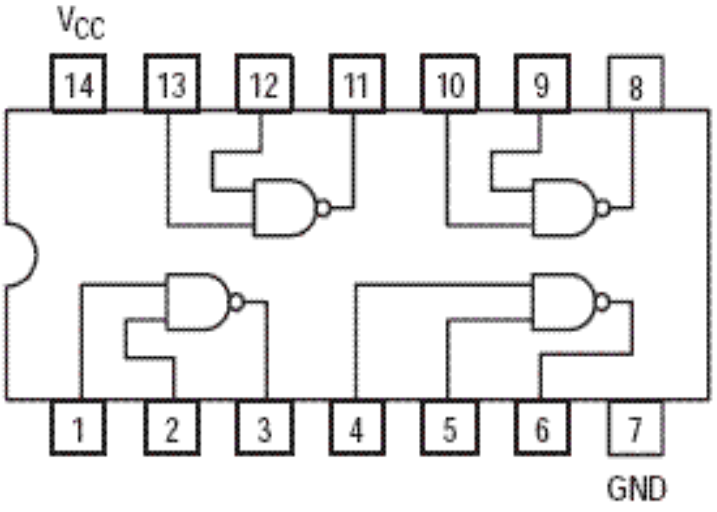
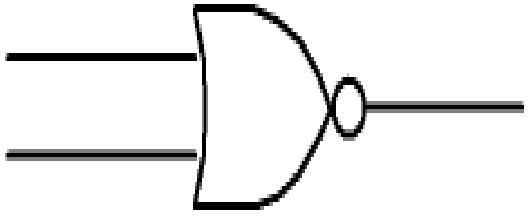


Fig1.4 LOGIC DIAGRAM OF NAND GATE IC 740

2 NOR: It is a combination of NOT and OR gate and the operation of NOR gate is inverse of the OR gate. Logical NOR operation is defined as "Its output only be at "1" when all its inputs are also at "0" otherwise its output will be "0".
Logical equation of NOR
Y = complement (A+B)



Logic symbol of NOR gate

Truth Table for NOR operation

INPUTS	OUTPUTS
A B	Y
0 0	1
0 1	0
1 0	0
1 1	0

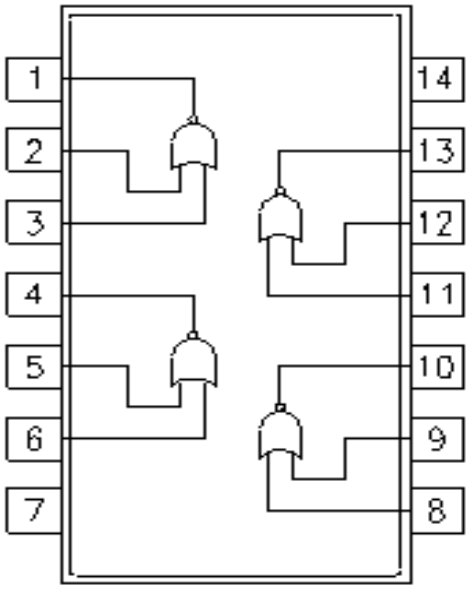


Fig1.5 LOGIC DIAGRAM OF NOR GATE IC 7402

EX-OR: Ex-or stands for exclusive OR. EX-OR gate counts the number of "1s" available at their inputs and if it is even number, the output is "0", and if it is odd number, the output will be "1"
Logical equation of EX-OR
Y =A'B+AB'

Logic symbol of EX-OR gate

INPUTS	OUTPUTS
A B	Y
0 0	0
0 1	1
1 0	1
1 1	0

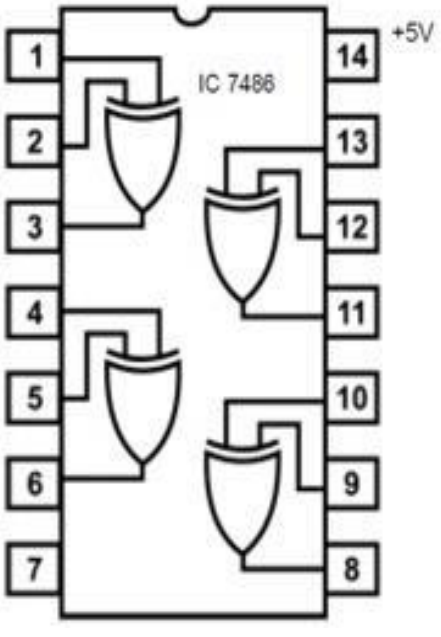


Fig 1.6 LOGIC DIAGRAM OF EX-OR GATE IC 7486

Procedure: -1) Apply Vcc to pin number 14 of all IC's & ground to pin number 7.
2) Assemble the circuit on breadboard according to the pin configuration.
3) Give the logical inputs and check for the proper output.
Conclusion: Hence verified the logical NAND, NOR, EX-OR Operation.

Exercise:

Q1. The inputs of a NAND gate are connected together. The resulting circuit is …….

1. OR gate
2. AND gate
3. NOT gate
4. None of the above

Q2. Digital circuit can be made by the repeated use of ……

1. OR gates
2. NOT gates
3. NAND gates
4. None of the above

Q3. The only function of NOT gate is to ……..

1. Stop signal
2. Invert input signal
3. Act as a universal gate
4. None of the above

Q4. The basic logic gate whose output is the complement of the input is …….

1. OR gate
2. AND gate
3. INVERTER gate
4. Comparator

Q5.When an input signal 1 is applied to a NOT gate, the output is ……

1. 0
2. 1
3. Either 0 & 1
4. None of the above

Q6. An OR gate has 4 inputs. One input is high and the other three are low. The output is …….

1. Low
2. High
3. alternately high and low
4. may be high or low depending on relative magnitude of inputs

Experiment No.2

Implementation of Boolean functions using Gates.

APPARATUS REQUIRED: Power Supply, Digital Trainer, IC's (7404, 7408, 7432) Connecting leads.
BRIEF THEORY: Karnaugh maps are the most extensively used tool for simplification of Boolean functions. It is mostly used for functions having up to six variables beyond which it becomes very cumbersome. In an n-variable K-map there are 2^n cells. Each cell corresponds to one of the combination of n variable, since there are 2^n combinations of n-variables. Gray code has been used for the identification of cells.
Example- f (A, B, C, D) =A'BC+AB'C+ABC'+ABC (SOP)
Reduced form is BC+AC+AB and POS form is f(X, Y, Z) = Y' (X'+Y+Z') (X+Z)

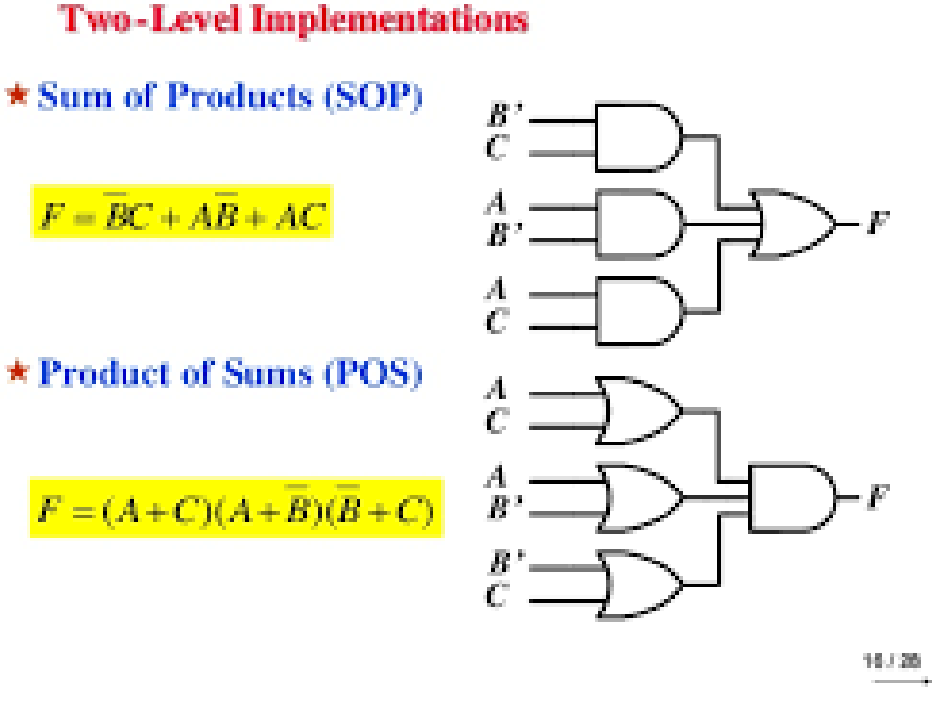


Fig.2.1 Logical Diagram

PROCEDURE:

(a) With given equation in SOP/POS forms first of all draw a K-map.

(b) Enter the values of the O/P variable in each cell corresponding to its Min/Max term.

(c) Make group of adjacent ones.

(d) From group write the minimized equation.

(e) Design the ckt. Of minimized equation & verify the truth table.

RESULT/CONCLUSION: Implementation of SOP and POS form is obtained with AND and OR gates.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.

2) The connections should be tight.

3) The Vcc and ground should be applied carefully at the specified pin only.

Exercise:

1. In a certain chemical processing plant, a liquid chemical is used in a manufacturing process. The chemical is stored in three different tanks. A level sensor in each tank produces a high voltage when the level of chemical in the tank drops below a specified point. design a circuit that monitors the chemical level and indicate when the level in any two of the tanks drops below the specified point. Draw the circuit using NANAD – AND two level implementation.

Solution:

Experiment No.3

Implementation of following code conversions:

A) **Binary to Gray B) Gray to Binary**

B) **Aim:-** To perform Binary to Gray Code Conversion

Apparatus: - Bread board, wires IC-7486(EX-OR)

Theory:-

Digital codes are required to handle data which may be numeric, alphabets or special characters. Since digital circuits work in binary manner, therefore numerals and other characters are to be converted to binary format. This conversion process is known as encoding.

Gray code:-

This code is often used in digital systems because it has the advantage that only one bit in the numerical representation changes between successive numbers. For example, 0111 represents 5 and 0101 represents 6 in Gray code .These two consecutive numbers differ only in one bit (third from left).Its primary application is in the location of angles on a rotating shaft.

Figure below shows circuit diagram of binary to gray code conversion & its truth table

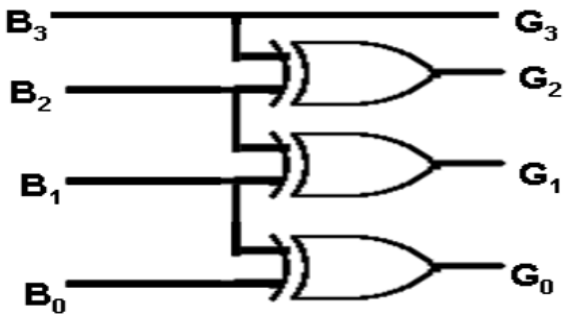


Fig 3.1 Circuit Diagram of Binary to Gray code Conversion

BINRY NUMBER S				CONVERTED GRAY CODE NUMBERS			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Procedure:-
1) Apply Vcc to pin number 14 of both IC's & ground to pin number 7 .
2) Assemble the circuit on bread board, as per above diagram.
3) Give the logical inputs and check for the proper output, as per the truth table.

Conclusion: Hence verified Binary to Gray code conversion operation

Aim:- To perform Gray Code to Binary Code Conversion

Apparatus:- Bread board , wires IC-7486(EX-OR)

Theory:-

Digital codes are required to handle data which may be numeric, alphabets or special characters. Since digital circuits work in binary manner, therefore numerals and other characters are to be converted to binary format. This conversion process is known as encoding.

Gray code:

This code is often used in digital systems because it has the advantage that only one bit in the numerical representation changes between successive numbers. For example, 0111 represents 5

and 0101 represents 6 in Gray code .These two consecutive numbers differ only in one bit (third from left).Its primary application is in the location of angles on a rotating shaft.

Figure below shows circuit diagram of gray code to binary conversion & its truth table.

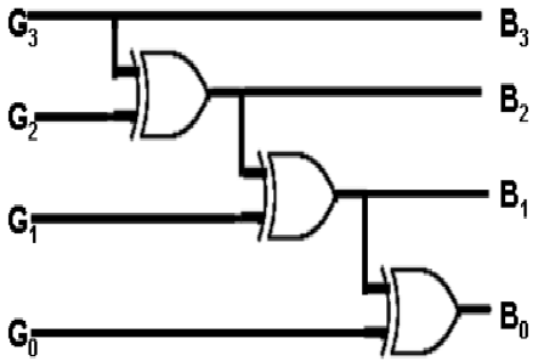


Fig 3.2 Circuit Diagram for Gray to Binary Conversion

Truth Table

GRAY CODE NUMBERS				**CONVERTED TO BINARY NUMBERS**			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Procedure:-

1) Apply Vcc to pin number 14 of both IC's & ground to pin number 7

2) Assemble the circuit on bread board, as per above diagram.

3) Give the logical inputs and check for the proper output, as per the truth table.

Conclusion: Hence verified Gray code to Binary conversion operation

Exercise: Explain any one practical application of gray to binary and binary to gray conversion.

Answer: Practical applications of Gray to Binary

Answer: Practical applications of Binary to Gray conversion

Experiment No.04

Implementation of Half adder and Full adder

(A) Study of Half Adder

Aim: To perform addition of binary digits using half adder circuit.

Apparatus: Bread board, wires IC-7486(EX-OR), 7408(AND)

Theory:-

A logic circuit for the addition of two one bit numbers is referred to as a half adder. A half adder can be constructed using EX-OR(IC-7486) and AND (IC7408) gates.

Figure below shows half adder circuit diagram & its truth table.

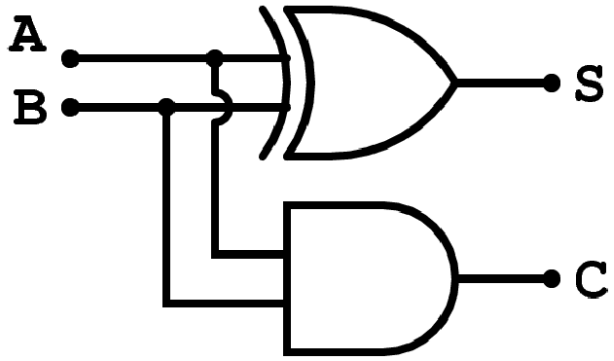


Fig 4.1 Circuit diagram of Half Adder

INPUT		OUTPUT	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The truth table shows, that in the first three rows there is no carry, whereas in the fourth row a carry is present.

From the truth table, we obtain the logical expression for SUM and CARRY as,

SUM=A'B+AB'

CARRY=AB

Procedure:-

1) Apply Vcc to pin number 14 of both IC's & ground to pin number 7 .

2) Assemble the circuit on bread board.

3) Give the logical inputs and check for the proper output.

Conclusion: Hence verified Half Adder operation

Exercise:

1. In parts of the processor, adders are used to calculate _____

   a)Addresses

   b)Table indices

   c)Increment and decrement operators

   d) All of the Mentioned

2. Total number of inputs in a half adder is _____

   a) 2

   b) 3

   c) 4

   d) 1

3. In which operation carry is obtained?

   a) Subtraction

   b) Addition

   c) Multiplication

   d) Both addition and subtraction

4. If A and B are the inputs of a half adder, the sum is given by _____

a) A AND B

b) A OR B

c) A XOR B

d) A EX-NOR B

5.The difference between half adder and full adder is _____

a) Half adder has two inputs while full adder has four inputs

b) Half adder has one output while full adder has two outputs

c) Half adder has two inputs while full adder has three inputs

d) All of the Mentioned

6. If A, B and C are the inputs of a full adder then the carry is given by _____

a) A AND B OR (A OR B) AND C

b) A OR B OR (A AND B) C

c) (A AND B) OR (A AND B)C

d) A XOR B XOR (A XOR B) AND C

7. How many AND, OR and EXOR gates are required for the configuration of full adder?

a) 1, 2, 2

b) 2, 1, 2

c) 3, 1, 2

d) 4, 0, 1

Experiment No.05

Study of Half Subs tractor

Aim:-To perform Subs traction of binary digits using half Subs tractor circuit.

Apparatus:- Bread board ,wires IC-7486(EX-OR),7408(AND)

Theory:-

A logic circuit for the subs traction of two one bit numbers is referred to as an Half Subs tractor. A Half Subs tractor can be constructed using EX-OR(IC-7486) and AND (IC-7408) gates. Figure below shows half Subs tractor circuit diagram & its truth table.

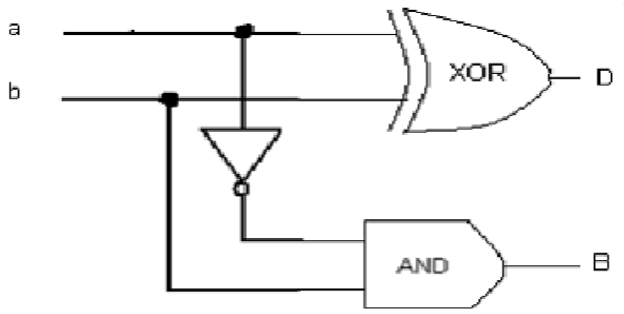


Fig 5.1 Circuit diagram of Half Subs tractor

INPUT		OUTPUT	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

The truth table shows, that in the first three rows there is no Borrow, whereas in the fourth row a Borrow is present.

From the truth table, we obtain the logical expression for DIFFERENCE and BORROW as,

Difference = A'B+AB'

Borrow = A'B

Procedure:-

1) Apply Vcc to pin number 14 of both IC's & ground to pin number 7 .

2) Assemble the circuit on bread board.

3) Give the logical inputs and check for the proper output.

Conclusion: Hence verified Half Subs tractor operation

Exercise:

Half sub tractor is used in ALU of processor, Justify your answer.

Answer:

EXPERIMENT NO: 06

Implementation of Multiplexer and De multiplexer

Aim:- To study Multiplexer operation using IC-74153
Apparatus: - Bread board, wires.
Theory:-
A Multiplexer (or a data selector) is a logic circuit that accepts several data inputs and allows only one of them at a time to get through to the output. The selection of the desired data input is controlled by the select (or address) inputs.
Figure below shows the block diagram of a Multiplexer.

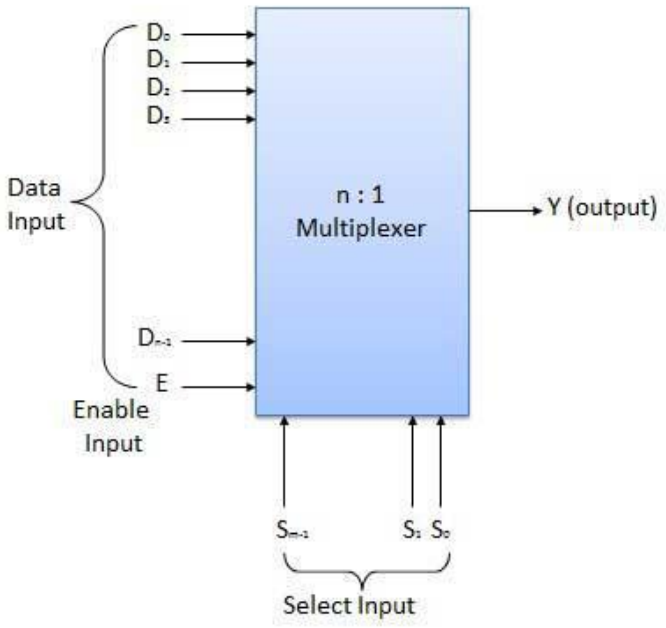


Fig 6.1 Block diagram of a Multiplexer

In this diagram the inputs and outputs are indicated by means of arrows . Depending upon the digital code applied at the SELECT inputs, one out of the data sources is selected and transmitted to the single output channel. The Multiplexer becomes enabled when the strobe signal is active LOW.
Note: - There are various Multiplexers available ex: 74151 (8:1), 74152--- etc. one can refer to data sheet for specification and pin Configuration

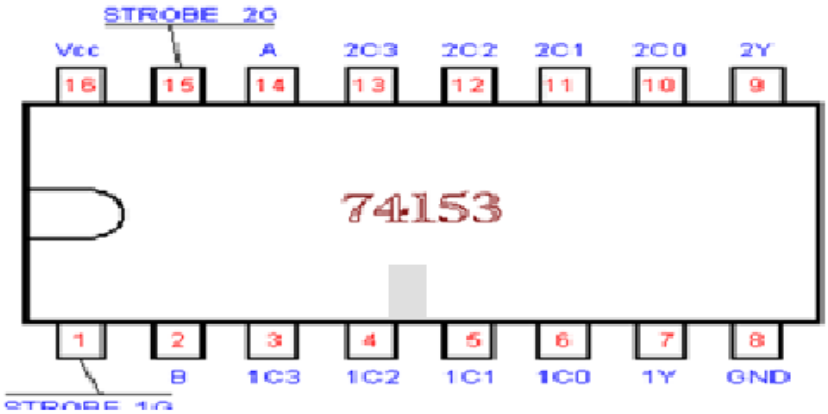


Fig. 6.2 IC 74153

Table 1 function table of IC 74153

Inputs							o/p
A	B	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

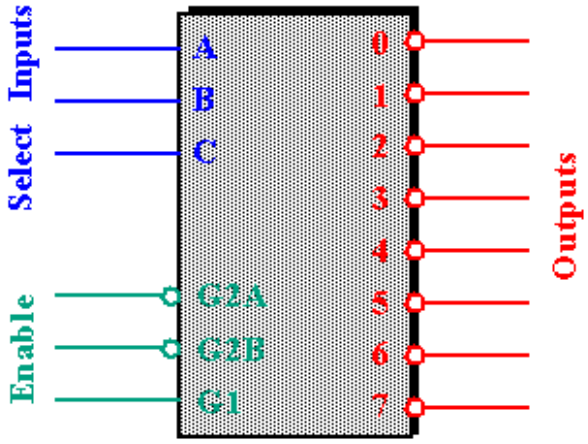
Procedure:-

1) Assemble the circuit on bread board, as per above diagram.
2) Give the logical inputs and check for the proper output, as per the truth table.

Conclusion: Hence verified the Multiplexer (4:1) operation using IC-74153

Aim: - To study Deultiplexer/Decoder operation using IC-74138
Apparatus: - Bread board, wires.
Theory:-
A Demultiplexer performs the reverse operation of a Multiplexer. It accepts a single input and distributes it over several outputs. The SELECT input code determines to which output the data input will be transmitted. The Demultiplexer becomes enabled when the strobe signal is active LOW.
This circuit can also be used as binary-to-decimal decoder with binary inputs applied at the select input lines and the output will be obtained on the corresponding line. These devices are available as 2-line-to-4-line decoder, 3-line-to-8-line decoder, 4-line-to-16-line decoder. The output of these devices is active LOW. Also there is an active low enable/data input terminal available

Figure below shows the block diagram of a Decoder.



Inputs						Output							
Enable			Select										
G2A	G2B	G1	C	B	A	0	1	2	3	4	5	6	7
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

Fig.6.4 4LS138 Decoder

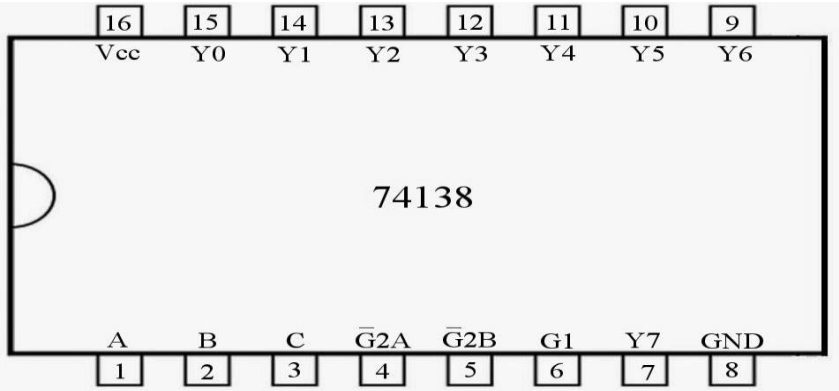


Fig 6.5 Pin diagram of a decoder 74LS138

Table 1 Function table of decoder 74LS138

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2} = \overline{G2A} + \overline{G2B}$

H = high level, L = low level, X = irrelevant

Depending upon the digital code applied at the SELECT inputs, one data is transmitted to the single output channel out of many.

Note: There are various Demultiplexers/Decoder available ex: 74156 1of 4 Decoder, 74139---etc one can refer to data Sheet for specification and pin Configuration

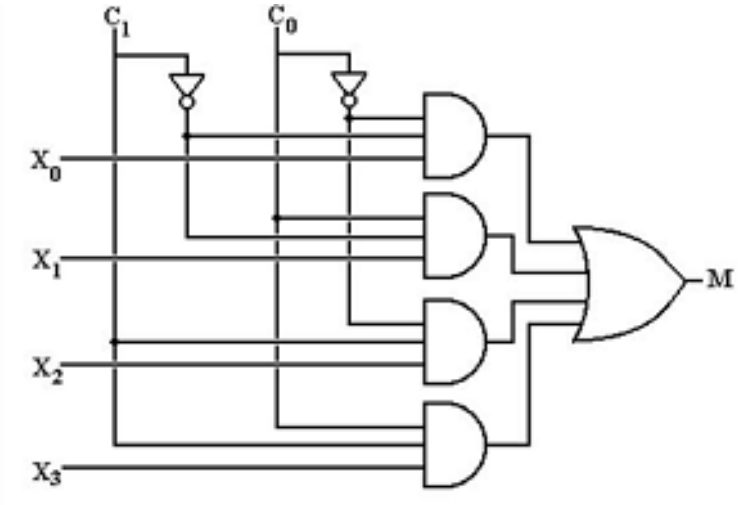
Procedure:-

1) Assemble the circuit on bread board, as per above Pin diagram.
2) Give the logical inputs and check for the proper output, as per the function table.

Conclusion: Hence verified the decoder (8::1) operation using IC-74138

Exercise:

In the given 4-to-1 multiplexer, if c1 = 0 and c0 = 1 then the output M is _____



a) X0

b) X1

c) X2

d) X3

JUSTIFY YOUR ANSWER.

_____

_____

_____

_____

_____

_____

_____

_____

_____

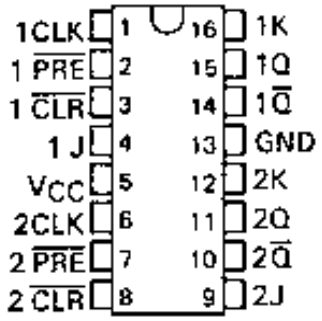
EXPERIMENT NO: 07

Study of flip flops

a) **J-K flip flops**
b) **D flip flops**
c) **T flip flops**

Aim:- To verify truth table for JK .D and T flip-flop.
Apparatus:- Bread board , wires .IC 7476(JK flip-flop),IC7474(D flip-flop)
Theory:-
1 Explain operation of SR flip flop, master slave JK flip flop with diagram.
2 Explain race around condition.
3 Draw symbols of JK, SR, D, T Flip Flops with truth tables

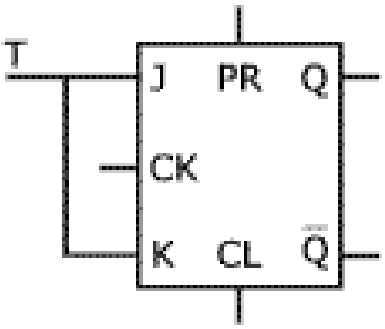
SN5476, SN54LS76A . . . J PACKAGE
SN7476 . . . N PACKAGE
SN74LS76A . . . D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	⊓	L	L	Q_0	$\bar{Q}_0$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

Fig 7.1 pin diagram and Function table of 7476



JK Flip Flop as T Flip flop

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

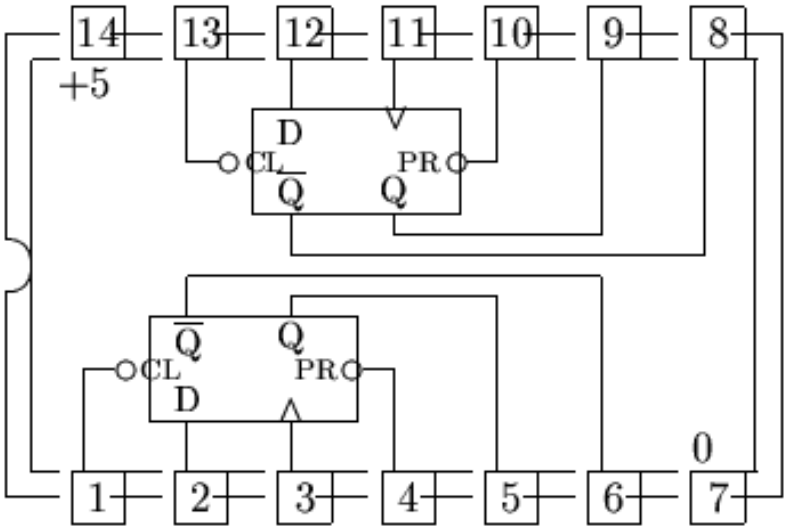
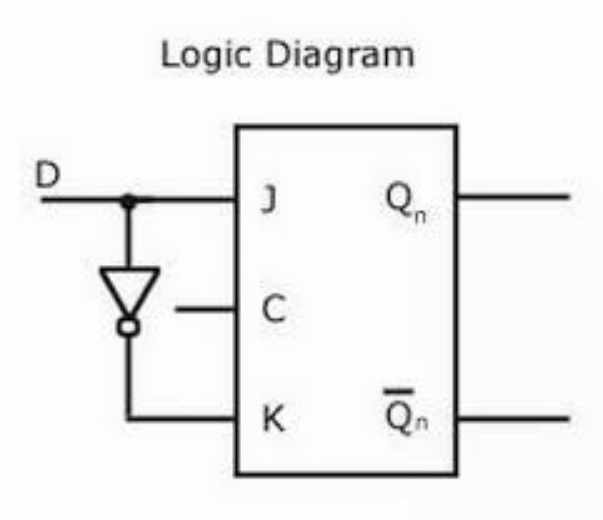


Fig 7.2 Function table and pin diagram of IC 7474 D flip flop



JK Flip-Flop as D flip flop

Procedure:-

1) Assemble the circuit on bread board, as per Pin diagram.
2) Verify operation of flip flops according to function /truth table

Conclusion: Hence verified flip flop operation using IC 7476 and IC 7474

Exercise

What are the roles of Flip flop in RAM (Random Access Memory)

EXPERIMENT NO: 08

Aim: To study Decade Counter using IC-7490
Apparatus: - Bread board, wires.
Theory:
A circuit used for counting the pulses is known as a Counter. Basically there are two types of counter:
1. Asynchronous counter (ripple counter)
2. Synchronous counter

In case of asynchronous counter all the flip-flops are not clocked simultaneously, whereas in a Synchronous counter all the flip-flops are clocked simultaneously. A Ring counter and twisted ring counter is the examples of synchronous counter.

Figure below shows the internal structure of 7490

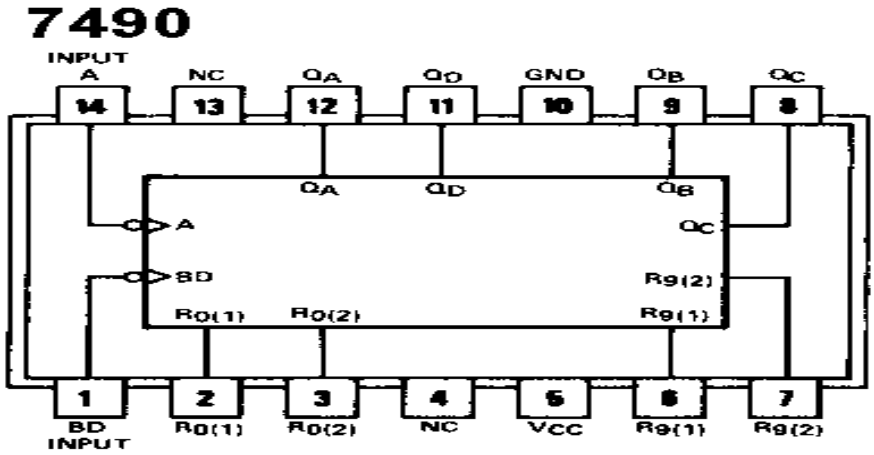


Fig.8.1 IC 7490

It consists of four flip-flop internally connected to provide a mod-2 and a mod-5 counter. The mod-2 and mod-5counters can be used independently or in combination. There are two reset inputs R0(1)and R0(2) both of which are to be connected to logic 1 level for clearing all the flip-flops. The two inputs R9 (1) and R9(2) when connected to logic 1 level, are used for setting the counter to 1001.

Table 1 count sequence

COUNT	QD(11)	QC(8)	QB(9)	QA(12)
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Procedure:-

1) Assemble the circuit on bread board, short Pin no.12 and 1
2) Give the Clock/trigger signal manually or auto clock at pin no.14 and check the count sequence.

Conclusion: Hence, studied the decade counter using IC-7490

Exercise:

List three applications of decade counter.

Answer:

1._____
_____
_____
_____
_____

2._____
_____
_____
_____
_____

3._____
_____
_____